

# Analysis of process parameters in “Smart Cut” SOI Structure fabrication

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## Abstract

*We have investigated Smart Cut process parameters for SOI structure fabrication. Oxidized silicon samples were implanted with  $H^+$  at 30, 40 and 60keV, with doses ranging from 1 to  $20 \times 10^{16} \text{ cm}^{-2}$ , followed by various annealing schemes. Optical microscopy (OM), transmission electron microscopy (TEM), and atomic force microscopy (AFM) were employed in the analysis of samples. Experiments reveal that a threshold dose for cavity formation resides between 3 and  $5 \times 10^{16} \text{ cm}^{-2}$  for hydrogen implantation through 100-200nm thermal oxides and energies ranging from 30 to 60keV. The product time-temperature rather than a critical temperature seems to be an important parameter in the layer splitting process. Top layer splitting was only obtained when slowly ramping up the temperature from room up to around 500°C during RTP annealing of wafer pairs. All cavities observed in TEM micrographs near the split surface have similar geometry, with a thickness around 3nm or ~20 atomic planes.*

## 1. Introduction

The increasing interest in new ways of obtaining compliant substrates arises as a consequence of common difficulties encountered when growing thin epitaxial films on relatively thick substrates, with mismatch in lattice parameters and temperature expansion coefficients.

The “Smart Cut” technology [1] that consists in layer transfer from a hydrogen implanted wafer onto a desirable substrate by wafer bonding and layer splitting is an attractive approach to form SOI (silicon-on-insulator) and other material combinations.

Fully depleted (FD) MOS transistors fabricated on SOI wafers will probably become one of the key technologies for volume production in the next years, specially for low voltage, low power applications due to their intrinsic advantages over bulk MOS devices [2].

## 2. Smart Cut Process

The Smart Cut technology has been well described in the literature [3,4]. It utilizes hydrogen ion implantation (I/I) through a thermally grown oxide to form buried cavities in a Si wafer [5-10], around the implantation projected range ( $R_p$ ). The use of I/I provides the required uniformity to the top Si thickness. The implanted wafer is then bonded at room temperature to either a bare or a thermally oxidized Si wafer and then annealed at mild temperatures (400-600°C) to promote coalescence of  $H_2$  filled cavities, hence wafer cutting, or splitting. This forms a SOI structure with a handle wafer (the unimplanted wafer from the pair), bonded thermally grown oxides and a cap Si layer. Once the SOI structure is formed, thermal annealing at higher temperatures (>1000°C) increases the bonding strength and improves the material quality and a final touch polishing renders a mirror like surface, suitable for the fabrication of ULSI circuits.

## 3. Experiments, Results and Discussion

We have performed a variety of experiments to determine optimum conditions for layer transfer and SOI structure formation.

Throughout this work we used cleaved fourths of CZ, p-type, (100), 8-12 $\Omega$ cm, 4" silicon wafers. Although wafer cleavage should affect negatively the bonding process, it was primarily necessary due to limitations in our furnace tube diameter and implantation equipment.

### 3.1. Implantation dose

Four different experiments were performed to determine an optimum range for the hydrogen implantation dose.

#### 3.1.1. Experiment 1

The first experiment included hydrogen I/Is through a 100nm thick thermal oxide, with variable doses in a large

range. The main objective was to narrow down the possible optimum range of doses to form internal cavities, also referred to as blisters when they reach the surface due to their appearance when the surface of a single implanted wafer is examined in an OM.

These cavities had recently been correlated to the Smart Cut internal splitting process to form SOI structures [11,12], with the formation of visible blisters taking approximately  $1/10^{\text{th}}$  of the annealing time to promote layer splitting at the same temperature.

Implantation energy of 30keV was used for an approximated projected range of 270nm from the Si/SiO<sub>2</sub> interface. The I/I doses were chosen so that the peak concentration would be around  $1.2 \times 10^{22}$  ions/cm<sup>3</sup>, according to Monte Carlo simulations with SRIM-2000.

Initially, we kept a fixed thermal treatment scheme in a Rapid Thermal Annealing (RTP) furnace, at 500°C for 30s, performed approximately 30h after the I/I. Similar annealing procedure of hydrogen implanted Si wafers had rendered significant increase in resistivity that was correlated to the presence of buried cavities [9].

Visual inspection in an optical microscope has shown that samples implanted with doses  $5.0 \times 10^{16}$  cm<sup>-2</sup> or higher formed superficial blisters, indicating that similar doses would probably also promote internal splitting of layers in SOI fabrication process.

Apparently, no blisters had been formed in samples implanted with  $3.0 \times 10^{16}$  cm<sup>-2</sup> or lower. On the other hand, the sample implanted with  $5.0 \times 10^{16}$  cm<sup>-2</sup> contained a reasonable density of blisters that although visible, had not blown up as in samples implanted with higher doses. These results show that the minimum dose for cavity formation ranges from  $3.0$  to  $5.0 \times 10^{16}$  cm<sup>-2</sup>.

### 3.1.2. Experiment 2

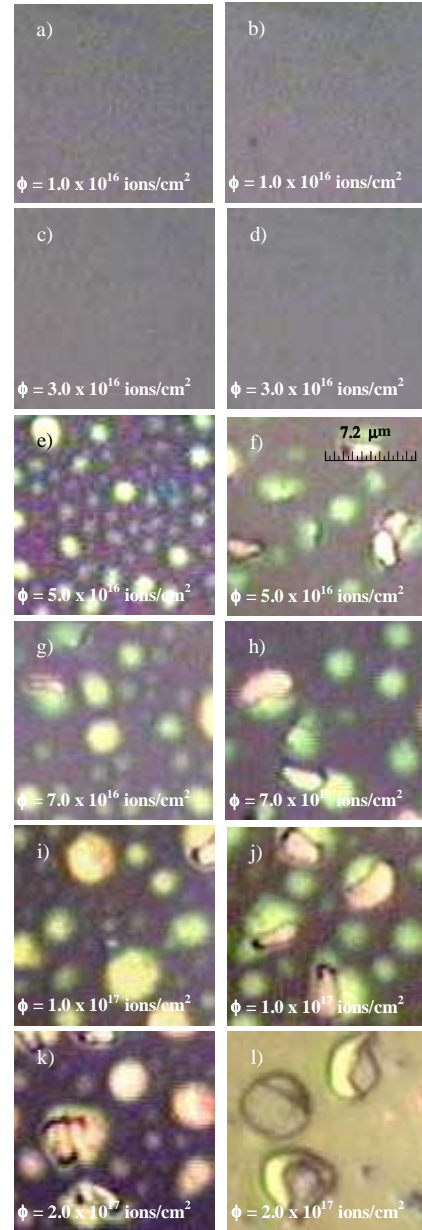
A second experiment was conducted with wafers equally covered with a 100nm thick thermal oxide and identical I/I and annealing parameters. The only difference was that the annealing was conducted 180h after the I/I instead of 30h as in the previous experiment. Fairly similar results to the ones from the previous experiment confirm that the vast majority of H<sup>+</sup> ions is effectively trapped in crystal defects due to I/I damage, losing the ability to freely diffuse through the wafer with regular rates. Therefore, a long time between I/I and annealing procedures does not cause any loss of hydrogen that could reduce the cavity density and, as a result, the ability to separate the thin top layer of Si from the rest of the wafer in the Smart Cut SOI structure formation process.

### 3.1.3. Experiment 3

Subsequently, we kept the same I/I doses as in previous experiments but increased the energy to 40keV.

Fig. 1 shows micrographs of sample surfaces, obtained in an optical microscope for wafers implanted at 40keV as an example of the results obtained in this and preceding experiments. Images on the left were taken for samples annealed in RTP at 500°C for 30s in N<sub>2</sub> environment whereas the ones on the right were taken for the same samples after conventional annealing at higher temperatures (next experiment). Again, samples

implanted with doses of  $5.0 \times 10^{16}$  cm<sup>-2</sup> and higher showed presence of superficial blisters and those implanted with  $3.0 \times 10^{16}$  cm<sup>-2</sup> or less have shown no blister formation when annealed at 500°C for 30s.

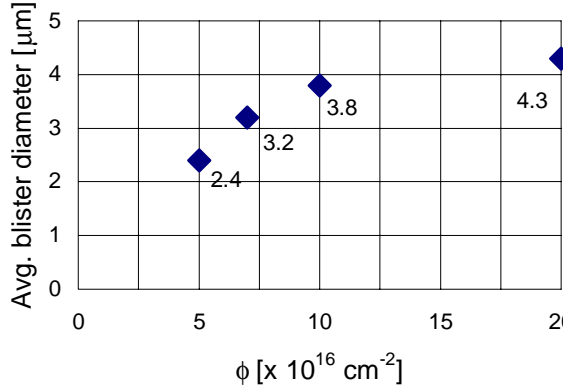


**Fig. 1 Optical microscopy surface images of hydrogen implanted samples after thermal annealing in RTP (left) and RTP + conventional (right).**

The I/I energy apparently plays only a minor role in the cavity formation process in the energy range evaluated (30 to 40keV) since no significant difference was noticed between previous experiments, where I/I was performed at 30keV and here, with 40keV, all other parameter kept fixed. However, higher energies imply deeper projected range, therefore cavities buried deeper in the wafer. As a consequence, longer times are necessary to form visible cavities at annealing temperatures below ~500°C as will be shown later. Above 500°C, however, no perceptible difference was noticed and it has been proposed that the

cavity formation kinetics does not depend on the implanted energy when wafers are annealed at temperatures above 500°C [13].

Analysis of images on the left side of Fig. 1 indicates a clear correlation between blister average diameters and I/I doses ranging from  $5.0 \times 10^{16} \text{ cm}^{-2}$  to  $1.0 \times 10^{17} \text{ cm}^{-2}$ . However, although we have doubled the dose from 1 to  $2.0 \times 10^{17} \text{ cm}^{-2}$ , Fig. 1 (i, k), the average diameter increased only slightly from 3.8 to  $4.3 \mu\text{m}$  as shown in Fig. 2 that plots the average blister diameter versus hydrogen I/I dose.



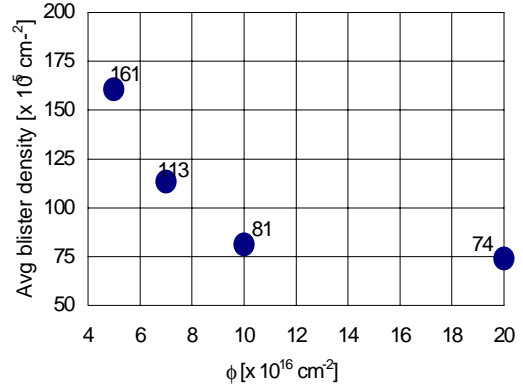
**Fig. 2 Average blister diameter as a function of  $\text{H}^+$  I/I dose.**

Specialized literature theorizes that part of the implanted hydrogen outdiffuses from the wafer, even at room temperature, when high doses are implanted [15]. Moreover, this reference determines  $1.6 \times 10^{17} \text{ cm}^{-2}$  implanted at 40keV as the maximum threshold above which internal splitting would not occur. Our results, with saturation in average blister diameters as doses are increased above  $1.0 \times 10^{17} \text{ cm}^{-2}$ , are compatible with that theory.

It is of paramount importance that both wafer surfaces are sufficiently flat and smooth for a high strength bond to occur between the pair. When wafers are implanted with doses as high as  $2.0 \times 10^{17} \text{ cm}^{-2}$  blisters become visible in an OM even before high temperature annealing. Such surface deformations would most certainly impair the ability to laterally grow cavities to promote their coalescence. A weak bonding strength due to surface non-uniformity will allow more blister formation and eventually wafer pair separation instead.

Lower values of dose produce internal microscopic defects and no superficial roughness increase is observed before annealing in agreement with [14].

On the other hand, there is an inverse correlation between density of blisters and dose as seen in Fig. 3 that plots the average blister density versus I/I dose. Apparently, as blisters grow and blow up, they consume part of the hydrogen from smaller blisters, or hydrogen filled cavities, annihilating some of them.



**Fig. 3 Average blister density as a function of  $\text{H}^+$  I/I dose.**

### 3.1.4. Experiment 4

The last experiment with multiple doses involved annealing in conventional furnaces of the same samples previously annealed in RTP. Images on the right side of Fig. 1 show the results obtained after annealing the samples from the left side at 700°C for 1h in  $\text{N}_2$ . Figures (b) and (d) show no blister formation for low I/I doses ( $< 3.0 \times 10^{16} \text{ cm}^{-2}$ ), even after annealing at high temperatures for a relatively long time. Also, notice that blisters in samples implanted with doses  $5.0 \times 10^{16} \text{ cm}^{-2}$  and above tend to increase and blow up after high temperature annealing. Again, this increase in blister size comes with the reduction in the density of small blisters (see Fig. 1 e-l). Once again, the sample implanted with the highest dose ( $2.0 \times 10^{17} \text{ cm}^{-2}$ ) shows a slightly different behavior, with a substantial reduction in density of small blisters. We believe that the presence of various blown up blisters already present in the very beginning of the conventional thermal treatment provide path for hydrogen loss. Therefore consuming it from smaller blisters and internal hydrogen filled cavities whose size reduction decrease the system's Gibbs free energy.

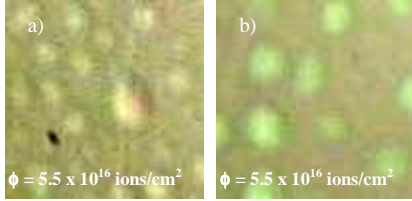
The initial experiments have shown us so far that the minimum necessary dose to promote blister formation, and probably layer splitting, is around  $5.0 \times 10^{16} \text{ cm}^{-2}$ , in agreement with other published works. Higher doses require shorter annealing time to form surface blisters. However, they also tend to form sparse larger blisters and, as a consequence, to increase the surface roughness that will reduce the bonding strength of wafer pairs in the SOI structure fabrication process and eventually prevent the internal layer splitting [14].

Therefore, it seems advisable to keep the I/I dose near the minimum necessary to promote blistering (and splitting).

### 3.2. Experiments with selected dose

Following a procedure similar to that of previous experiments, we implanted samples with  $\text{H}^+$  at 40keV to a dose  $5.5 \times 10^{16} \text{ cm}^{-2}$  through a 200nm thick thermal oxide. We selected a dose that is only slightly above the minimum in order to promote internal splitting and yet not too high to keep high bonding strength. Fig. 4 shows micrographs obtained for a sample annealed in RTP at 500°C for 30s (a) and the same sample after annealing at

700°C for 1h (b). As expected, the results are similar to the ones in previous experiments, with the same behavior for size and density of blisters before and after the conventional annealing. Also, the presence of blisters indicates the dose is appropriate to promote internal splitting for SOI structure formation as confirmed in later experiments.



**Fig. 4 OM surface images of hydrogen implanted samples. (a) After annealing in RTP and (b) RTP + conventional furnace.**

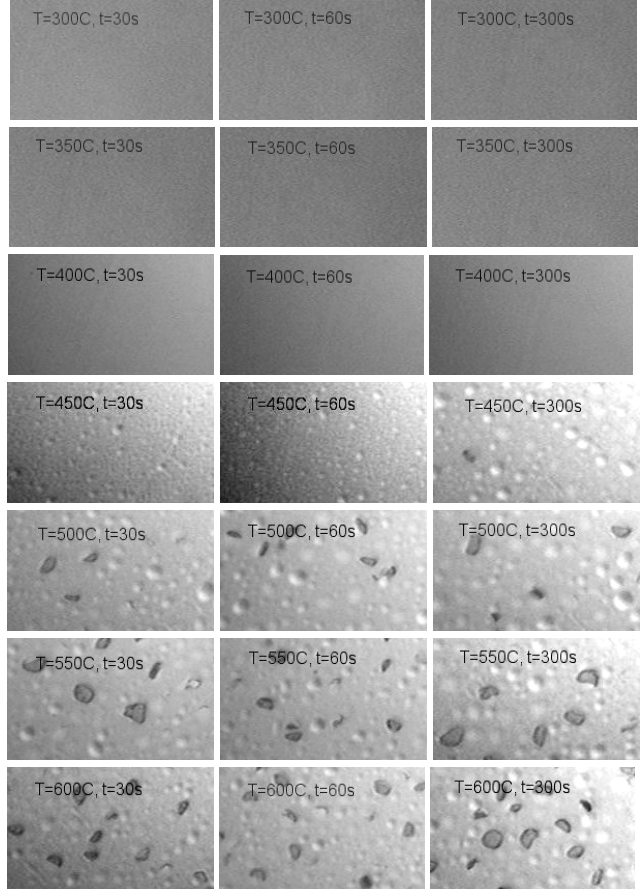
### 3.3. Time for blistering

Two experiments were performed to determine the time required to form optically detectable surface blisters with 40 and 60keV of I/I energy. All samples were with a dose of  $5.5 \times 10^{16} \text{ cm}^{-2}$  through a 200nm thermal oxide.

#### 3.3.1. Time for blistering-40keV

A number of implanted samples were annealed at various combinations of temperature and time in order to map the necessary time for blistering as a function of temperature. Samples were implanted at 40keV and subsequently annealed in an RTP furnace ( $\text{N}_2$ ) at temperatures ranging from 300°C to 600°C, with 50°C steps, for 30s, 60s or 300s, generating a total of 21 samples. The micrographs in Fig. 5 show surface images with a magnification of approximately 2000X, registered for each one of them with an optical microscope.

Notice that blisters are present only for samples annealed at temperatures higher than 400°C for all time intervals. Samples annealed at 450°C show very few blisters when annealed for 30s, with blister density increasing with annealing time. Also for this annealing temperature, the average blister diameter is approximately  $1.1\mu\text{m}$  for samples annealed for 30s and 60s but with an increased density in the sample annealed longer. For the sample annealed for 300s, we notice a significant increase in blister diameter, with an average of  $1.7\mu\text{m}$ , and a slight increase in density. The significant increase in blister diameter with annealing time occurs for all temperatures. Blister diameters also increase with increasing temperature. An increase in average diameter from  $1.7\mu\text{m}$  to  $1.9\mu\text{m}$  is observed when comparing samples annealed at 450°C with that annealed at 500°C, both for 300s. Only a marginal increase in diameter when going from 500°C to 550°C and no perceptible increase when going from 550°C to 600°C.



**Fig. 5 OM surface images of hydrogen implanted samples with  $5.5 \times 10^{16} \text{ cm}^{-2}$  at 40keV through 200nm-oxide layer, after thermal annealing.**

We also see a relatively high density of blown up blisters from 500°C and above, in agreement with other published results [11,15]. The increase in blown up blisters comes in the expense of size and density of smaller blisters. More blisters blow up as the annealing time and temperature increase. The average size of blown up blisters is  $1.3$  to  $2.5\mu\text{m}$  in our experiments, similar to the  $2.0$  to  $3.0\mu\text{m}$  range reported in [15] for a non oxidized sample.

A careful analysis of the images shows that the size and density of blisters for one sample at a certain temperature correspond to similar values in samples annealed at higher temperatures for shorter periods. This suggests that the product *time x temperature* rather than a critical temperature is the important parameter in the blister formation kinetics.

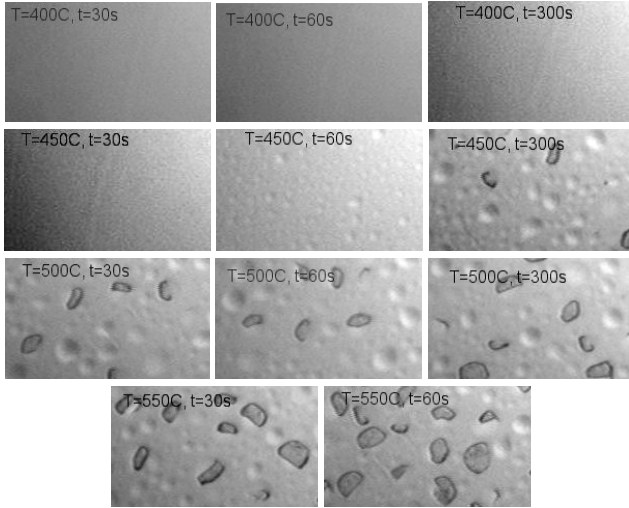
#### 3.3.2. Time for blistering -60keV

In a new evaluation of the effect of the I/I energy, we partially reproduced the previous experiment, only increasing the I/I energy to 60keV. The annealing temperature was varied from 400°C to 550°C in 50°C steps and the annealing times were kept unaltered.

Again, our results were very similar in all aspects: threshold temperature for blister formation, their size and evolution, and density of blown up blisters as clearly seen in Fig. 6.

A notable difference was that samples annealed for 30s at 450°C have no clearly visible surface blisters. Again, this result suggests that energy plays a secondary role in the cleavage process, if all other conditions are maintained the same.

As previously mentioned, higher energies imply deeper projected range, therefore cavities buried deeper in the wafer. As a consequence, longer times are necessary to form visible cavities.



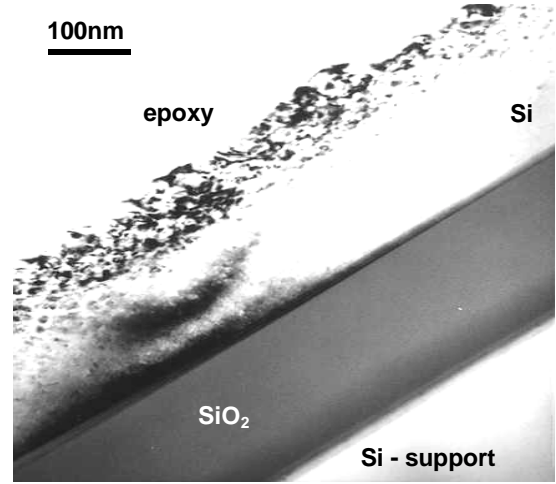
**Fig. 6 OM surface images of hydrogen implanted samples with  $5.5 \times 10^{16} \text{ cm}^{-2}$  at 60keV through 200nm oxide layer, after thermal annealing.**

### 3.4. SOI structure

Our early experiments showed that although it is relatively easy to obtain a bonded pair with unimplanted wafers, I/I of  $\text{H}^+$  into one of them imposes new obstacles to be overcome. For instance, after I/I the Si surface becomes hydrophobic, which is known to reduce the room temperature wafer bonding strength. Also, if the bonding strength is not sufficiently high, cavities grow into blisters, instead of laterally coalesce with other neighbor cavities as desired in the splitting process [15].

New samples of silicon wafers were implanted at 40keV with  $5.5 \times 10^{16} \text{ cm}^{-2}$  through a 200nm thick thermal oxide and then bonded to other unimplanted and oxidized (200nm) silicon wafers. Subsequently, each bonded pair was annealed in RTP ( $\text{N}_2$ ) to promote splitting of the top layer of the implanted wafer, rendering the SOI structure. The annealing temperature was ramped up from room temperature to around 500°C in approximately 200s.

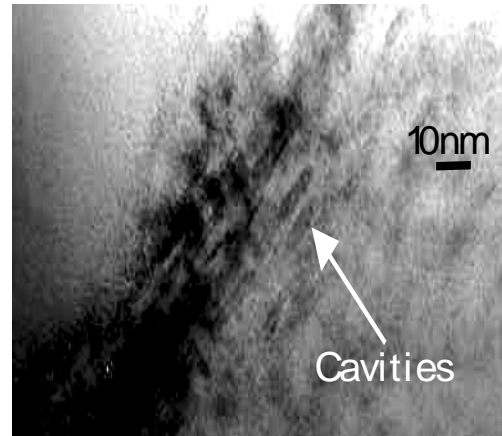
TEM samples were prepared out of the SOI structure formed to examine the thickness of the various layers as well as the possible presence of defects in the top Si layer. The TEM micrograph in Fig. 7 clearly shows the SOI structure, with a 480nm silicon layer on top of a 400nm buried oxide. About 320nm of the transferred silicon layer is crystalline, with no visible defects, covered by an amorphous layer, as revealed by the diffraction pattern of that region.



**Fig. 7 Cross-sectional transmission electron micrograph of the SOI structure.**

Close inspection of the amorphous or highly defective region, shows the presence of several cavities that were formed away from the splitting plane. The TEM micrograph of Fig. 8 clearly shows the presence of cavities, detected by verifying the contrast change from dark to bright Fresnel fringes when going from under-focus to overfocus conditions. Interesting to notice is that all visible cavities are similar in size and shape, with 25nm of lateral length extension along (001) planes and a constant thickness (in [001] direction) of about 3nm or ~20 atomic planes.

Fig. 9 shows a two-beam condition [ $g = 220$ ] cross-section micrograph at a higher magnification, taken from the defective region, where it is possible to notice the presence of defects oriented along (001) and (111) planes. Planar defects along (111) planes might nucleate inclined cavities with respect to the (001) surface orientation and eventually increase the surface microroughness [16].



**Fig. 8 Two-beam, cross-sectional, bright field transmission electron micrograph in slight under focus condition.**



**Fig. 9** Cross-sectional transmission electron micrograph with (001) and (111) planar defects.

MFA analysis allowed for the observation of the surface morphology and revealed a 5.8nm RMS roughness in an average from 14 measurements in a scanned area approximately  $400\mu\text{m}^2$ .

#### 4. Conclusion

Our experiments reveal that the threshold dose for cavity formation resides between  $3.0$  and  $5.0 \times 10^{16} \text{ cm}^{-2}$  for hydrogen I/I through 100-200nm thermal oxides and energies ranging from 30 to 60keV.

Apparently the product *time x temperature* rather than a critical temperature is the important parameter in the blister formation, or splitting process kinetics.

Hydrogen filled cavities grow and induce in-depth splitting of the implanted wafer during annealing if bonded to an unimplanted handle wafer or surface blistering in isolated wafers. Top layer splitting for SOI structure formation was only obtained when wafer pairs were annealed in RTP, slowly ramping up the temperature from room up to around  $500^\circ\text{C}$  in a couple of minutes.

We have also noticed that all cavities observed in TEM micrographs near the split surface have similar geometry, with a thickness (in [001] direction), around 3nm or  $\sim 20$  atomic planes.

In summary, a SOI structure has been obtained by the combination of close to optimum parameters found in our experiments.

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#### References:

- [1] M. Bruel, *Electron. Lett.*, **31**, 1201, (1995)
- [2] J. P. Collinge, "SOI Technology: Materials to VLSI", Kluwer Academic Publishers, Boston (1991)
- [3] M. Bruel, B. Aspar, B. Charlet, C. Maleville, T. Poumeyrol, A. Soubie, A. J. Auberton-Hervé, J. M. Lamure, T. Barge, F. Metral, and S. Trucchi, 1995 IEEE International SOI Conference Proceedings, 178 (1995)
- [4] A. J. Auberton-Hervé, J. M. Lamure, T. Barge, M. Bruel, B. Aspar, J. L. Pelloie, "SOI Materials for ULSI Applications", *Semiconductor International*, October, 97, (1995)
- [5] C. C. Griffioen, J. H. Evans, P. De Jong, and A. Van Veen, *Nucl. Instrum. Methods*, B **27**, 417 (1987)
- [6] S. M. Myers, D. M. Follstaedt, H. J. Stein, and W. R. Wampler, *Phys. Rev. B*, **45**, 3914 (1992)
- [7] C. H. Seager, S. M. Myers, R. A. Anderson, W. L. Warren, and D. M. Follstaedt, "Electrical Properties of He-implantation-produced nanocavities in silicon", *Phys. Rev B*, **50**, 2458 (1994)
- [8] R. Siegele, G. C. Weatherly, H. K. Haugen, D. J. Lockwood, and L. M. Howe, "Helium bubbles in silicon: Structure and optical properties", *Appl. Phys. Lett.* **66** 1319 (1995)
- [9] J. Li, "Novel semiconductor structure formed by hydrogen implantation", *Appl. Phys. Lett.*, **55**, 2223 (1989)
- [10] F. F. Morehead and B. L. Crowder, *Radiat. Eff.*, **6**, 27 (1970)
- [11] Q. Y. Tong, T. H. Lee, K. Gutjahr, S. Hopfe, and U. Gösele, "Layer splitting process in hydrogen-implanted Si, Ge, SiC, and diamond substrates", *Appl. Phys. Lett.*, **70**, 1390 (1997)
- [12] Q. Y. Tong, T. -H. Lee, L. -J. Huanh, Y. -L. Chao, and U. Gösele, "Si and SiC layer transfer by high temperature hydrogen implantation and lower temperature layer splitting", *Electronics Letters*, **34**, No. 4, 407, (1998)
- [13] B. Aspar, C. Lagahe, H. Moriceau, A. Soubie and M. Bruel, "Kinetics of Splitting in The Smart Cut® Process", in *Proceedings of the IEEE International SOI Conference*, 99 (1998)
- [14] M. Bruel, B. Aspar, and A. J. A. Hervé, "Smart-Cut: A New Silicon On Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding", *Jpn. J. Appl. Phys.*, **36**, 1636, (1997)
- [15] X. Lu, N. W. Cheung, M. D. Strathman, P. K. Chu, and B. Doyle, "Hydrogen induced silicon surface layer cleavage", *Appl. Phys. Lett.*, **71**, (1997)
- [16] Q.-Y. Tong, R. Scholtz, U. Gösele, T.-H. Lee, L. -J. Huang, Y. -L. Chao, and T. Y. Tan, "A 'Smarter-Cut' approach to low temperature silicon layer transfer", *Appl. Phys. Lett.*, **72**, (1998)