TEOS SiO_2 films deposited at low temperature

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Introduction

Silicon oxide is widely used in thin film technologies. PECVD, using TEOS, is a well known technique to deposit SiO_2 thin films [1]. We are developing SiO_2 thin films deposition process to be applied as well in integrated technology for metal interlevel dielectrics as in large area technology for gate oxide of thin film devices.

Experimental

The PECVD home made cluster tool system, used in this study, was described elsewhere [2]. Silicon wafers (100), p-type, 10-20 Ω.cm, 75 mm in diameter were used as substrate. The experiments were carried out using a gas mixture of TEOS and oxygen in the basic following conditions: 5 sccm TEOS, 500 sccm O_2, wafer holder temperature 360°C, pressure 1 Torr, RF power 400W and distance between electrodes 15 mm. We analyzed the influence of RF power, wafer holder temperature and total pressure in deposited silicon oxide layer. MOS capacitors were implemented for electrical characterization.

Results and Discussion

The deposition and etching rates increase for RF power higher than 250 W. This behavior is explained by the high production of excited oxygen (O^*) in the reactor, as observed by OES analysis, which enhances the TEOS molecules oxidation. For RF power lower than 250 W, the energy of the plasma is too low to generate enough O^* [3].

The deposition and etching rates decrease with the wafer holder temperature. This behavior is typical of adsorption controlled reactions. An increasing of the temperature increases the kinetic energy of active species, which also increases the desorption probability and thus reduces the adsorption probability [4].

The etching rate increases with the pressure and reaches a maximum at around 2 Torr. This behavior can be explained by the variation in the gas flow regime in this pressure range. Considering the flux of gas mixture constant, when the process pressure is increased the mean free path of the molecules and gas velocity decreases, and the residence time increases, so interactions between the species in the gas phase are improved.

When the gas velocity decreases the sub products of surface reaction can not be well removed, and some of them remain trapped inside the film. These sub products, as reported in the literature, are mainly Si-OH and –OH which enhance the silicon oxide etching rate [1].

MOS capacitors were implemented with silicon oxide film deposited in the basic condition. The silicon oxide layer was densified in an RTP furnace at 1100°C, 120 s. Table I summarizes the electrical parameters extracted from the C-V and the I-E curves. We observe that the value of dielectric constant (ε) decreases after annealing. This behavior can be explained by the presence of Si-OH and –OH contamination in the oxide layer. The value obtained for the densified sample, lower than that reported for thermal silicon oxide, may be explained by the presence of dangling bonds into the silicon oxide which was not completed during annealing.

Table I: Electrical Parameters

	As Deposited	Densified
Thickness (nm)	80	78
ε	4.35	3.53
V_{fb} (V)	-2.71	-0.99
N_{ss} (cm^{-2})	$5.36x10^{-11}$	$1.45x10^{-10}$
$I_{leakage}$ (A)	$4x10^{-10}$	$1.7x10^{-11}$
E_{bd} (MV/cm)	9.0	10.5

The densification step improves the electrical characteristics of the silicon oxide film, which is attributed to the elimination of trapped charges by the thermal treatment. These charges are produced during the deposition process due to the sub-products of the TEOS oxidation.

Conclusion

The RF power enhances the O* generation in the plasma increasing the TEOS oxidation process in the gas phase. Also, the oxidation reaction and sub products elimination, from the surface during solid phase reaction, are improved. The wafer holder temperature contributes to the volatile sub products elimination from the substrate surface. There is no evidence of Si-OH and OH bonds in the FTIRS spectra from the films deposited above 300°C. We observed a decreasing in the dielectric constant (ε) after annealing, due to the presence of Si-OH and –OH contamination in the oxide layer. This contamination is below the detection limit of the FTIRS analysis technique. The densification process improved the electrical characteristics of the film showing an elimination of trapped charges promoted by the thermal treatment.

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