EVOLUTION OF RELIABILITY ASSESSMENT IN PCB ASSEMBLIES

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Abstract

Very low failure rates, down to 10 FIT are now currently expected by electronic system manufacturers. In the same time, severe conditions of utilisation are common in most of industrial and commercial applications, like automotive sector for example. In order to assess this reliability “challenge”, process control, design and technological solutions have to be optimised to guarantee almost no defect during the operating life time. Reliability testing strategy must also strongly evolve from the classical accelerated ageing statistical median life testing to the use of more sophisticated degradation laws, based on physics of failure, and in many cases computer assisted.

1- Introduction

Electronic circuits are more and more used in mobile systems or non protected environments, where they are submitted to severe constraints. It is the case for example for automotive and mobile phone electronic boards which have to face harsh mission profiles where thermal cycling, vibrations, shocks, moisture and other chemical aggressions can be simultaneously present.

<table>
<thead>
<tr>
<th>Temp</th>
<th>Engine environment</th>
<th>Dashboard</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low(°C)</td>
<td>-40</td>
<td>-40</td>
</tr>
<tr>
<td>High(°C)</td>
<td>+85 to +125</td>
<td>+85</td>
</tr>
<tr>
<td>ΔT(°)</td>
<td>125 to 165</td>
<td>125</td>
</tr>
<tr>
<td>Typ Nb per year</td>
<td>750</td>
<td>750</td>
</tr>
<tr>
<td>Chemical aggression</td>
<td>Moisture Others</td>
<td>80% at 40°C 98% at 40°C</td>
</tr>
<tr>
<td>Mechanical stresses</td>
<td>Vibrations</td>
<td>1 to 2 kHz 20 to 40 Hz</td>
</tr>
</tbody>
</table>

Table 1 - An example of automotive circuit mission profile

As an example, we have reported on table 1 an example of « mission » envelope frequently encountered in this type of application. As electronics is now involved in nearly all human activities, the reliability concern has indeed become a major one, conditioning personal safety, economic efficiency and product marketing. However, the near-zero failure objective, combined to the high complexity of circuits and harder mission profiles have requested a complete change in reliability approach. Tight process control, very short reaction loops, accurate strength-load analysis are now essential conditions to hope for good reliability results, all of them being based on physics modelling of defects and degradation phenomena. The development of semiconductor IC technology, driven by the constant demand of the market, is characterised by an increasing complexity. This fact has to be integrated in packaging technology, by larger I/O capacity, increased electrical performances, and also by a constant tendency to more miniaturisation. One of the consequences of this rapid evolution is the coexistence of many different packaging technologies on a same board, as represented on figure 1 where CSP (Chip Size Package), TSOP (Thin Small Outline Package) and PBGA (Plastic Ball Grid Array) are frequently assembled on a same board.

![Fig. 1: Mobile phone main board with different packaging technologies](image_url)

Reliability of SMT (Surface Mounting Technology) is a critical concern for equipment manufacturers. Very high levels of reliability, around 10 FIT, (1 FIT represents 1 failure in 10^9 device hours) are required in most industrial applications; this objective is very difficult to obtain, especially due to the fact that an assembled board is the result of many different technological processes, including IC foundry, packaging process, passive components manufacturing and assembling process. All these processes are generally performed independently, so that defect density and failures can be cumulative and compatibility problems can easily appear.
2- Components reliability evolution

Over the three last decades, IC manufacturing progress in defect reduction (figure 2) was obtained by a rigorous process control at each step of the process.

Fig. 2 : Defect reduction (right side scale) and life operating failure rates (left side scale) estimation for IC manufacturing for the last thirty years

Wafer yield and defect density connection were many twice established, as pointed out for example by Gerling [1] and by Kuper and Van der Pol [2]. Early failure (EL) rates down to 10 ppm are now achieved with yield in the range of 80%; with 98% yields, some manufacturers have been able to claim near-zero EL failure. This strong reduction of defect density in silicon IC technology is also related to the constant improvement of end of life reliability (EOL) as shown on the estimation drawn in figure 2. Failure rates down to 10 FIT and even less are commonly expected by manufacturers and required by many sectors of application, such as automotive industry, aeronautics and also by traditional high reliability electronic systems for medical and space applications, etc.

Table 2 - The relation between volume, process control and reliability for IC manufacturing

<table>
<thead>
<tr>
<th>Volume (million/year)</th>
<th>&gt;100</th>
<th>&lt;1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cpk</td>
<td>1.5 to 2</td>
<td>1 to 1.3</td>
</tr>
<tr>
<td>Yield (%)</td>
<td>85 to 98</td>
<td>40 to 60</td>
</tr>
<tr>
<td>Burn-in (hr)</td>
<td>~0</td>
<td>48 to 168</td>
</tr>
<tr>
<td>Reliability (Fits)</td>
<td>0.1 to 10</td>
<td>100 to 1000</td>
</tr>
</tbody>
</table>

Table 2 shows an analysis performed by A. Jonath and R. Thomas [3] where the relationship between volume, yield and reliability results are highlighted. The process capability Cpk is the quality indicator commonly used by semiconductor manufacturing, where deviations from a reference value for different critical parameters are expressed as a function of σ, the gaussian standard deviation. High volume and mature VLSI productions reach Cpk up to 2. Clearly, 1 to 10 FIT can only be obtained through highly controlled processes. Very high yields can also lead to a drastic reduction of burn-in since the defect density inducing EL failure have been almost removed. Some DRAM and other high volume/well matured technologies are announced to be produced without burn-in because of potential defect generation during this selection test. Yield improvement can be achieved through many factors, one of the main being high volume production, which allows WLR (Wafer Level Reliability) analysis and SPC (Statistic Process Control) procedures.

WLR test structures are commonly used to check metal/dielectric integrity, hot carrier susceptibility, oxide breakdown and degradation, ESD effects, metal interconnection, electromigration and stress voiding etc. Besides defect reduction, yield and EL failure improvement, WLR leads to a better in-operation reliability evaluation of the product.

SPC and also the emerging field of data mining [4] are essential tools for yield and reliability improvement, because they are keys to control and to improve the dispersion of critical technological parameters.

Let us give the example shown on figure 3 related to the influence of parameter dispersion on electromigration ageing behaviour. From the classical Black law describing both temperature and current density effects on electromigration failure,

\[ t_f = A J^{-n} \exp \left( \frac{E}{kT} \right) \]  

we have introduced a distribution of interconnection thickness. Assuming arbitrarily an instant failure \( t_f \) at \( 10^6 \) hours for the mean value of the thickness distribution, the influence of parameter dispersion clearly appears in the Weibull diagram of figure 3, by a difference in the slope \( \beta \) of the cumulative failure function. Values of \( \beta \) larger than 10 are indicators of rather well controlled processes with respect to the corresponding defect generation.

For PCB (Printed Circuit Boards) assemblies, the reliability goals are similar to those of semiconductor manufacturing, since most of IC are incorporated in packages and then in boards. The problem, from a system point of view, is to keep an equivalent degree of
process control in packaging, passive component manufacturing, and in board assembling. As mentioned in the introduction, reliability assessment is complicated by the number of different processes leading to a PCB assembly, increasing in particular technological interfaces. Nevertheless, levels of 10 FIT are also expected at least by packaging and assemblies large manufacturers for high volume and mature technologies, with methods similar to those developed in IC foundries. Due to the difficulty to implement WLR strategy like for silicon components, product inspection remains for packaging and assemblies a very important step. Powerful analysis techniques allow detection and localisation of defects using non-destructive operation. X-ray microfocus and ultrasonic low frequency microscopy are dedicated to solder cracks, package-chip interface etc. detection and location. X-ray laminography is particularly well adapted to derive geometric fluctuations of soldering process in production environment.

An example of good process control consequence on reliability is given on figure 4 corresponding to a power IGBT half bridge module [5]. It can be noted after a Weibull analysis from the cumulated failure probability measurement that most of failures are concentrated after 70,000 power cycles on a short time range, which guarantee a very low failure rate in the operational life of the system.

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The strength-load approach

However, process dispersion is obviously not the only factor which controls reliability in electronic devices. Load distribution, issued from the spreading of stresses applied to the component in its mission profile has also a major influence. The strength-load approach has recently been well developed by Jensen [6]. It gives a good idea of the device robustness. The crossing between the highest stresses values of the mission profile and the low side of strength distribution tail results in the occurrence of failure (figure 5).

For every critical technological parameter, the strength-load relationships is of course determined through degradation law where stressing factor influences, such as temperature, humidity, voltage ones etc., are related to the device attributes, all of them being represented by a distribution function.

3- Fast analytical evaluation of assembly criticality

However, specific questions are arising, especially due to the fact that for a given electronic function, many packaging and assembling solutions are offered. Technological choices must take into account the stress profile of the application. Accelerated ageing tests for all configurations become rapidly cost dissuasive, so that board designers ought to have convenient tools to evaluate the criticality of different configurations with respect to main constraints and to make a first selection. Important concerns for a lot of applications are the susceptibility to thermomechanical and delamination phenomena.

Thermomechanical susceptibility

Soldering between package and board is especially affected by thermal cycling, so that joints in leaded or unleaded packages are in many case a critical part of the assembly.
and packages, on the package size and on lead stiffness. In BGA technology, the poor compliance of the balls makes the assemblies critical to thermal cycling as soon as large size and CTE mismatch are combined. An illustration of these technological features, joint to the characteristics of the load cycles (thermal amplitude, dwell time and total number of cycles) is represented on the diagram of figure 7 where two cases are considered. The first one corresponds to a non critical assembly using a small dimension plastic BGA package with a low CTE mismatch with the substrate. The second one, a large ceramic BGA package, is more subjected to thermomechanical stresses.

**Fig. 7 : Thermomechanical behaviour of two different assemblies: a large ceramic BGA --- and a small plastic BGA --- reported on FR4.**

To go further in thermal cycling susceptibility modelling, FEM (Finite Element Model) simulation performed on several cycles can be used in order to correlate the assembly configuration with the maximum plastic strain in the most sensitive region of the package. However, if this technique gives excellent results for strain or stress mapping, it takes too long time for a first selection. In this case, the analytical approach remains a good alternative, even if the model uses strong simplifying hypothesis (balls are assimilated to cylinders). Following this line, the thermomechanical criticality can be evaluated from the calculation of strain for a given ΔT, measured at the package corner (figure 8) farthest from the symmetry centre. The largest approximation is that no plastic strain is considered in the lead or in the ball, which is physically wrong in most cases but sufficient to estimate a comparative susceptibility. As shown on figure 8 for BGA, transverse and longitudinal displacements δ are calculated on the peripheral ball rank, following classical mechanics relations:

\[
\delta_i = \frac{F l^3}{3E_2 J}, \quad \delta_i = \delta_{i-1} - \frac{SL}{AE_1} + \alpha L \Delta t
\]

where \(\frac{F l^3}{3E_2 J}\) is the flexural deformation of the vertical column, \(\delta_{i-1} = \frac{SL}{AE_1}\) the compressive deformation of the horizontal beam, and \(\alpha L \Delta t\) its thermal dilatation. In these formulas, \(\alpha\) is the differential dilatation of the assembly (\(\alpha = \alpha_{\text{case}} - \alpha_{\text{substrate}}\) ), \(E_1\) the Young modulus of the case, \(E_2\) the Young modulus of the solder, \(A\) the section of the horizontal beam, \(l\) the height of the column and \(J\) its moment of inertia, \(L\) the length of the beam (i.e. the pitch between two balls), \(\Delta T\) the temperature variation, \(F\) the force applied at the top of the column “i” and \(S\) the sum of the forces applied at the top of columns 1 to i.

This iterative calculation is done with MAPLE software, and needs to enter both geometric inputs (ball and package dimensions) and physical constants of the different materials (Young modulus, CTE).

**Fig. 8 : Simplified model of the assembly for the analytical calculation**

It can be noted that in the case of CSP (Chip Scale Package), where the proportion of moulding compound compared to the silicon chip area is more or less equivalent, it is also necessary to estimate the effective CTE of the package structure [7]. From the above calculation, we have developed a program which allows a quasi-instant comparison between different configurations, as shown on table 3 and 4.
Table 3 – Evaluation of the thermomechanical criticality using analytical calculation ($\delta$) and FEM simulation ($\Delta\gamma$) of 3 configurations with ball solder joints reported on a FR4 PCB

<table>
<thead>
<tr>
<th>Package</th>
<th>$\delta$ (µm)</th>
<th>$\Delta\gamma$ ($10^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBGA 352</td>
<td>0.46</td>
<td>4.7</td>
</tr>
<tr>
<td>CSP48</td>
<td>0.4</td>
<td>3.4</td>
</tr>
<tr>
<td>PBGA192</td>
<td>0.3</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Table 4 – Evaluation of the thermomechanical criticality using analytical calculation (F) and FEM simulation ($\Delta\gamma$) of 3 leaded packages reported on FR4 PCB

<table>
<thead>
<tr>
<th>Package</th>
<th>F (N)</th>
<th>$\Delta\gamma$ ($10^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSOP44</td>
<td>310x10^{-3}</td>
<td>14</td>
</tr>
<tr>
<td>PQFP80</td>
<td>8.4x10^{-3}</td>
<td>3</td>
</tr>
<tr>
<td>SOJ40</td>
<td>4.3x10^{-3}</td>
<td>2.9</td>
</tr>
</tbody>
</table>

Table 5 - Evaluation of delamination susceptibility from analytical calculation. $\sigma$ is the resin tensile stress and $\tau$ is the chip/substrate shear stress

<table>
<thead>
<tr>
<th>Package</th>
<th>$\sigma$ (Mpa)</th>
<th>$\tau$ (Mpa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBGA 352</td>
<td>22</td>
<td>5</td>
</tr>
<tr>
<td>TQFP 160</td>
<td>20</td>
<td>4.5</td>
</tr>
<tr>
<td>SOJ 36</td>
<td>13</td>
<td>1.2</td>
</tr>
<tr>
<td>HQFP 240</td>
<td>15</td>
<td>7</td>
</tr>
</tbody>
</table>

**Delamination susceptibility in plastic packages**

As shown by Casasnovas and al [8] in an experimental analysis, another frequent type of defect encountered in plastic packages is related to delamination formation under mechanical stresses appearing at interfaces between assembled materials.

In order to establish a fast classification of plastic packages with respect of constraints in the resin-chip-leadframe systems, Hy Vay Cai [9] has proposed a program based on the following relations. The first one is proposed by Olsen et al [10]:

$$\sigma_p = \frac{(\alpha_p - \alpha_c)(T_g - T)E_p}{E_cA_c + E_pA_p}$$

This relation gives the overall tensile stress in the moulding compound, where $\alpha_p$, $E_p$ and $\alpha_c$, $E_c$ are the CTE and the Young modulus of the resin and of the chip, $T_g$ is the glass transition temperature in the resin, and $A_p$, $A_c$ the resin and chip section areas.

The second one [11] is addressing the shear stress $\tau(x)$ at the chip-leadframe interface, in the adhesive joint between these two last parts:

$$\tau(x) = \frac{\Delta T \cdot \Delta \alpha \cdot G \cdot \sinh(\beta \cdot x)}{\beta \cdot f \cdot \cosh(\beta \cdot L)}$$

with

$$\beta^2 = \frac{G}{t} \left[ \frac{1}{E_c h_c} + \frac{1}{E_p h_p} \right]$$

where $\Delta \alpha$ is the CTE difference, $G$ the adhesive shear modulus, $E_2$ the leadframe young modulus, $L$, $h$ the geometric dimensions of the assembly and $x$ the position from the symmetry centre. An example of comparative evaluation following these two types of stresses is given on table 5.

Note that the main use of this kind of analysis is to derive a comparative evaluation and to possibly point out a critical behaviour. The connection with failure delamination is conditioned to actual adherence measurements.
4 - Reliability testing

In the nineties, Crook [12] pointed out the problem of reliability testing on VLSI circuits when very low failure rates of 10 FIT and less have to be demonstrated through classical accelerated test on products. It must be borne in mind that acceleration factors of more than 400 are difficult to consider due to physical limitation in devices, in all cases limited in temperature, for example in plastic packages. Thus, the duration and the cost of testing is rapidly dissuasive, as shown in the figure 9, where classical temperature ageing testing at 125°C with a degradation mechanism governed by an activation energy of 0.6 eV was considered. Even when reducing the test duration to the occurrence of the first or the two first failures, the number of test samples become rapidly high if reasonable confidence level wants to be obtained. WLR tests structures are designed to enhance the susceptibility to the stress and thus allow higher values of acceleration factors [13].

![Sample size versus failure rate](image)

**Fig.9 : Sample size versus failure rate : test temp. 125°C, act. Energy 0.6 eV, Poisson distribution**

However, test sequences, even using WLR structures, are remaining costly and time consuming phases; reliability indicators may allow strong test time reduction by using specific measurements under “normal” operating conditions. It may also address very short accelerated loading conditions. In all cases the relations between the measured parameters (or set of parameters) and the failure threshold must have been identified through a preliminary study of failure modelling.

An example is given in figure 10 for a BCD (Bipolar, CMOS, DMOS) technology where gate oxide WLR control usually performed through TDDB analysis is proposed to be replaced by a single Fowler-Nordheim first current value [14].

![Indicator of TDDB analysis](image)

**Fig.10 : The use of early indicator to shorten dielectric qualification test in BCD technology [14]**

However, in the case of high cost devices or complex modules or hybrid microelectronic circuits, the number of samples under test can be dramatically low without possibility of acceleration factor increase. This situation leads to poor quality confidence levels in the data statistics. An improvement of data exploitation can be obtained using Monte Carlo method, by generating specified random parameters. Stochastic simulation by Monte Carlo method is helpful to obtain numerical results whenever a wide spread of empirical data, related to incomplete analytical models, are used to describe degradation laws and reliability functions. On the hypothesis of a given statistical distribution of failure times, a larger set of virtual devices is created; the distribution of the extrapolated lifetimes is then supposed representative of the behaviour of the actual samples as shown in the example of figure 11: from a short measurement duration, on a few DUT, an extended sample is simulated until failure times happen, in order to estimate the failures distribution p(t). Initially very little time-consuming, this simulation method may furthermore be parametrically enhanced whenever a new “real” data is obtained, reasons which explain the growing success of this approach.

![An illustration of reliability data processing by random generation](image)

**Fig.11 : An illustration of reliability data processing by random generation**
5- Computer assisted and generic reliability assessment of PCB assembly under thermal cycling

The main goal of this kind of accelerated testing is to ensure that the overall assembly design and manufacturing fits well the reliability requirement under operating conditions and that the product life is in agreement with the mission profile. The number of cycles to failure under thermomechanical stresses is traditionally described from the Coffin-Manson [15] [16] equation:

\[ N_f = \frac{1}{2} \left( \frac{\Delta \gamma}{2 \varepsilon_f} \right)^c \]  

(5)

where \( \Delta \gamma \) is the strain rate in the solder joint; the coefficients \( c \) and \( \varepsilon_f \) are related to the technology characteristics and the temperature conditions (Engelmaier [17]). It can be noted that the important parameter in the failure mechanism is in practice the local maximum elastic and plastic strain, because it leads to the crack initiation at a given region of the joint. The determination of local maximum \( \Delta \gamma \) can only be done using FEM (Finite Element Model) simulation mapping, as shown in figure 12 on a BGA ball. This simulation was performed with ANSYS software.

![Fig. 12: Maximum cumulated plastic strain mapping in half of the SBGA352/FR4 ball (ANSYS FEM simulation)](image)

On the other hand, the failure identification is usually done through the measurement of resistance change in a daisy-chained component which requires specific test samples and addresses only heavy degraded joints.

In order to have a better knowledge of the failure occurrence, it is interesting to perform a fast physical analysis of the joint and to observe directly the first microcracks on a standard operating component. Furthermore, a more accurate degradation law can be derived, in the case of Sn63Pb37 solder joint, by following the lead rich phase coarsening (figure 13).

![Fig. 13: Joint phase evolution coarsening mean surface for a CSP48/FR4 assembly from 0 to 1000 thermal cycles](image)

Using a fixed procedure, the increase in the mean surface of the lead phases is measured by SEM imaging in the most strained regions. This increase, observed on a cross section up to the apparition of cracks along the tin-lead area interface, leads to the following experimental law:

\[ \Delta S = A(\Delta \gamma)^\beta \left( N_c \right)^{\frac{1}{2}} \exp \frac{E_a}{kT} \]  

(6)

where \( A \) is a constant, \( E_a \) the activation energy of the degradation, \( \Delta \gamma \) is the maximum local plastic strain, \( N_c \) the number of cycles and \( t_p \) the dwell time at the upper temperature. Crack initiation appears when a limit value of \( \Delta S \) is reached. The exponent \( \beta \) is evaluated at around 0.5 for the technology under study.

Life testing using relation 6 needs both experimental ageing and FEM simulation to evaluate \( \Delta \gamma \) from the assembly configuration, as shown in figure 14; its value depends essentially on the CTE differential between materials and on the package size.

![Fig. 14: ANSYS simulated equivalent total strain stress curves for a CSP48/FR4 assembly](image)
The duration of ageing test can be adjusted to wait for the first crack initiation. It is also possible to use relation 6 as a continuous degradation phenomena, which of course leads to shorten strongly the stress duration, the phase coarsening law being then considered as a reliability indicator, for instance up to 300/400 cycles. However, this procedure should be available only if a stable soldering process can be guaranteed.

Table 6a gives a result of reliability qualification under accelerated ageing of 1000 cycles with an amplitude of -55°C/+125°C where the first cracks appeared. Using an expression of acceleration factor \( AF \) deduced from (6):

\[
AF = \frac{N_{c2}}{N_{c1}} = \left(\frac{\Delta Y_1}{\Delta Y_2}\right)^{\frac{1}{p_1}} \exp\left(\frac{2E_a}{k} \left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right)
\]  

(7)

This gives (table 6b) an equivalent operating number of 16000 cycles with an amplitude of 0°C/+80°C, not so far from, for example, the automotive dashboard conditions. For \( N_{c1} \) cycles in accelerated and \( N_{c2} \) in operational conditions, \( \Delta Y_1 \) and \( \Delta Y_2 \) are respectively the maximum plastic strain range, \( T_1 \) and \( T_2 \) the upper temperatures and \( t_{p1}, t_{p2} \) the cycles upper dwell times.

Table 6 - Qualification of different assembly configurations under thermal cycling using a generic accelerated test and FEM simulation

<table>
<thead>
<tr>
<th>Assembly</th>
<th>Conditions</th>
<th>( N_{c1} )</th>
<th>( N_{c2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) CSP48 FR4</td>
<td>Accelerated test (Generic) ( N_{c1} = 1000 ), -55°C + 125°C ( \Delta Y_1 = 3.4 \times 10^3 ), ( T_1 = 125°C )</td>
<td>1000</td>
<td>-</td>
</tr>
<tr>
<td>(b) CSP48 FR4</td>
<td>Expected Operational conditions ( 0°C + 80°C ), ( \Delta Y_2 = 4 \times 10^{-4} ), ( T_2 = 80°C, t_{p2}/t_{p1} = 10 )</td>
<td>-</td>
<td>16000</td>
</tr>
<tr>
<td>(c) PBGA192 FR4</td>
<td>Accelerated test (Virtual) ( -55°C + 125°C ), ( \Delta Y_2 = 1.5 \times 10^3 ), ( T_2 = 125°C )</td>
<td>2200</td>
<td>2200</td>
</tr>
<tr>
<td>(d) PBGA192 FR4</td>
<td>Expected Operational conditions ( 0°C + 80°C ), ( \Delta Y_2 = 1.5 \times 10^4 ), ( T_2 = 80°C, t_{p2}/t_{p1} = 10 )</td>
<td>-</td>
<td>44000</td>
</tr>
</tbody>
</table>

A PCB assembly is generally composed of many different package configurations, each of them having its own response to a stress solicitation. Taking into account that the common feature is the report process for all of them, it is thus interesting to derive from one only accelerated testing the potential reliability for all the packages reported on a board and, if necessary, for a same board in different operating conditions. For example the number of cycles capability of PBGA192 assembly, is given on table 6c and 6d, from the previous accelerated testing, considered as generic for this report process, and from a \( \Delta Y \) ANSYS evaluation corresponding to the specific configuration.

Furthermore, with the recent development of process control including SPC, data mining, and other specific indicators, it is now possible to improve the reliability value of physical degradation laws, like for example relation 6, by introducing process fluctuation distributions. An illustration of that it is called “virtual qualification” can be found in reference [18], on a topic also directly related to PCB assemblies reliability evaluation. Coming back to the strength-load representation, a further step will be to include in the degradation model the structural weakening which generally results from ageing. In this case, reliability simulation will be certainly in the good way.

6- Conclusions

Very low failure rates for electronic devices are now commonly required for many applications, and this evolution towards very high reliability levels is strongly pushed by the market. High volume semiconductor industry has improved manufacturing yields and besides the gain in production efficiency, defect density reduction and weak parametric dispersion have positive effects on component reliability. Reliability assessment of electronic assemblies is facing specific difficulties: one is due to the number of possible different packaging technologies and packaging size configurations which can be assembled on a same board. Fast analytical evaluation of susceptibility with respect to major sources of failures, such as weld crack initiation or interface delamination, can be a good tool to perform the best selection, which can simplify the qualification procedures. Degradation modelling through physics of failure is also of course one of the main basis for high reliability assessment, through shortening accelerated ageing tests from reliability indicators. Associated FEM simulation allowing to take into account size and other configuration parameters are very useful to simplify tests files and may reach to generic tests, particularly interesting in a board where many different encapsulation technologies are present. Finally, the availability of data with respect to different processes or other manufacturing parameter dispersion can be incorporated in the degradation laws to derive a more realistic description of failure distributions.
Acknowledgements:

We would like to thank M. Barré Matra Bae Dynamics (France), R.W. Thomas from Technology Experts Network (USA), A. Touboul University of Bordeaux (France), O. Bonnaud, University of Rennes (France), for the fruitful discussions with them.


