IMPROVED CURRENT MIRROR OUTPUT PERFORMANCE BY USING GRADED-CHANNEL SOI NMOSFETS

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Abstract

This work introduces the use of Graded-Channel SOI MOSFETs to make analog current mirrors and compare their performance with those made with conventional fully depleted SOI transistors.

It is demonstrated that Graded-Channel MOSFETs can provide higher precision current mirror with enhanced output swing.

Also lesser modifications of the output characteristics due to the self-heating effect than in conventional SOI MOSFET have been observed.

1. Introduction

The advantages of fully-depleted (FD) Silicon-On-Insulator CMOS technology in comparison to bulk Si regarding analogue circuit design have been reported in [1] for the first time. Most of them relate to the combination of the reduced capacitance of SOI technology with the better transconductance (g_m) over drain current (I_{DS}) ratio due to the reduced body factor of FD transistors, which provides enhanced bandwidth and gain, resulting in very significantly improved micropower CMOS OTAs (operational transconductance amplifiers)[1].

However, due to the presence of a parasitic bipolar transistor with floating base, FD devices may suffer from output impedance degradation due to the low drain breakdown problem [2]. This parasitic bipolar action is more pronounced at gate voltages close to the threshold voltage.

One of the most important building blocks for analogue circuit operation is the current mirror (CM), which is typically used to actively bias or load analog circuit branches. Ideal CM operation presupposes to deliver an output current (I_{OUT}) identical to the input current (I_{IN}), independently of the output transistor drain bias (V_{DSout}), i. e. the ratio $R=I_{OUT}/I_{IN}$ should be as close to unity as possible.

Due to the output impedance reduction, the performance of CM made using FD devices may be significantly degraded, mainly in moderate and weak inversion regimes, which are of major interest to increase the output swing in low voltage operation. Several solutions have been successfully proposed such as series-parallel association of transistors (2). However, the major drawback of this approach is the severe increase in the total amount of required die area.

The Graded-Channel SOI MOSFET (GC) is an asymmetric channel device which has been introduced recently with the aim to reduce the inherent parasitic bipolar effects of SOI devices (figure 1) [3-4]. An undoped region is preserved in the drain side of the channel , i. e. the threshold voltage implant is not performed in this region, reducing the amount of majority carriers generated by impact ionization, which drive the base current of the parasitic bipolar structure associated to the MOSFET.

In addition, the presence of a strong depletion region in the low doped region makes the electric field in the transition of the implanted/unimplanted parts of the channel only very slightly dependent on the drain bias, which results in a very low channel length modulation. GC transistors indeed demonstrated enhanced drain breakdown voltage, superior transconductance in saturation and significantly reduced drain output conductance [5]. This undoped region presents negative threshold voltage and can be considered as an extension of the drain region (through the inversion layer) below the gate. Thus, in a first

approximation, the device effective channel length (L_{eff}) can be estimated as the difference between the mask channel length (L) and the length of the undoped region (L_{LD}) [3].

Regarding the analog circuit design, previous works indicate that GC transistors can appreciably improve the DC gain and unity-gain frequency allowing the realization of high-gain wide-bandwidth OTAs while reducing the required die area[4].

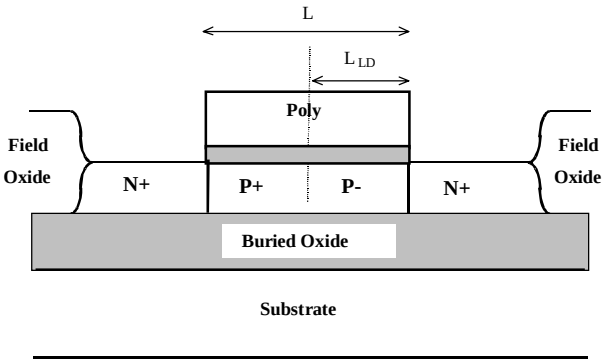

Figure 1. Cross section of the Graded Channel SOI nMOSFET.

The goal of this work is to introduce the use of GC SOI MOSFET to make current mirrors and to compare its performance with those made with conventional FD transistors.

2. Device Characteristics and Measurements

Common-source CM designed using both GC and FD devices were simultaneously processed on Smartcut wafers, according to the 2 µm process described in [3]. The final thicknesses of the gate oxide, silicon film and buried oxide are 30 nm, 80 nm and 390 nm, respectively. In the case of the GC CM, the ratio L_{LD}/L has been varied by photolithographic masking during the channel implantation to verify its impact on the output performance. It should be emphasized that slight mask misalignment will not significantly affect GC CM performance since it can easily be made equal for both input and output transistors by symmetric design. Both FD and GC CM were designed following the same layout.

Figure 2 shows the measured I_{DS}/W (W being the channel width) against drain voltage (V_{DS}) characteristics, obtained at a gate voltage overdrive V_{GT}=150 mV, for both individual GC (W/L=18µm/2µm and several L_{LD}/L) and FD transistors (W/L=20µm/1µm and 18µm/2µm) indicating the improvement in output conductance for similar effective channel length.

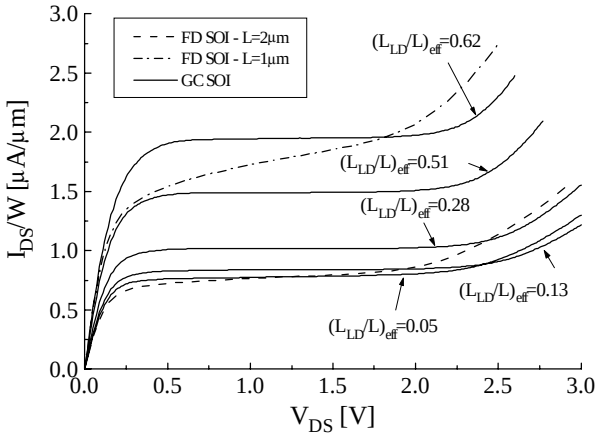

Figure 2. Measured I_{DS}/W against V_{DS} curves (V_{GT}=150 mV) for the GC and FD devices.

An evaluation of the Early voltage (V_{EA}) variation as a function of the inversion level is presented in figure 3, which plots the extracted V_{EA} as a function of the normalized drain current ($I_{DS}/W/L_{eff}$) for the GC and FD transistors with similar mask channel length. Such curve has been obtained by biasing the transistors with the gate and drain electrodes connected. This way, the devices are kept in saturation in all regimes of inversion.

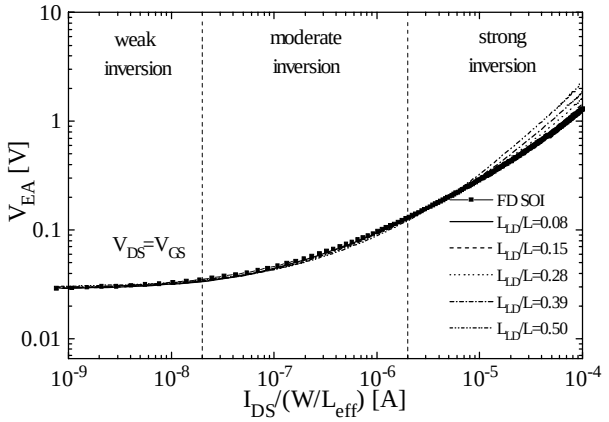

Figure 3. Measured V_{EA} as a function of the normalized drain current for the GC and FD devices in all regions of operation.

The Early voltage is the same for all transistors in both weak and moderate inversion and GC transistors only increase the Early voltage in strong inversion. However, as current mirrors are generally biased in strong inversion, the benefits of using GC are maximized.

Figure 4 plots the R ratio as a function of the normalized input drain current ($I_{Dsin}/(W/L_{eff})$), where W is the device channel width, for the several fabricated CM with GC and FD devices, both with W/L=18/2 and measured at V_{DSout}=1.5 V. Such curve has been obtained by varying I_{IN} (1nA≤I_{IN}≤1mA), in order to cover all regions of operation. This graph also includes a FD CM with L=4 µm.

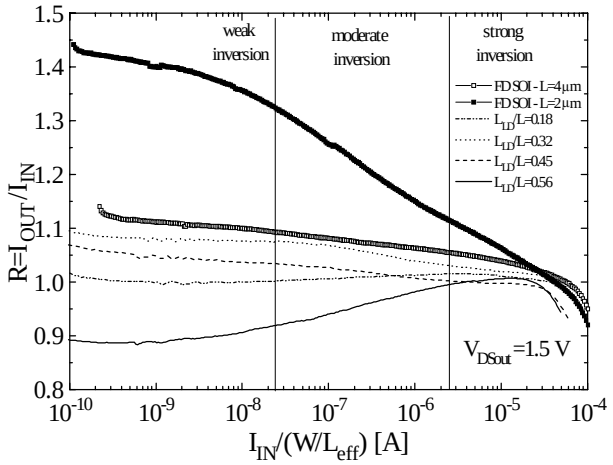

Figure 4 – Measured output to input ratio (V_{DSout}=1.5V) as a function of the normalized input drain current.

In order to better correlate the results and verify the transistor mismatch influence, the results of figure 4 are plotted in figure 5, as a function of the input transistor drain-to-source potential drop (V_{DSin}). this curve also clearly shows that the GC configuration improves the CM output performance. The bold dotted lines on the figure indicate the CM biased in nominal condition, i. e. V_{DSout}=V_{DSin}. In this condition, if there is no transistor mismatch, the R ratio must be equal to unity.

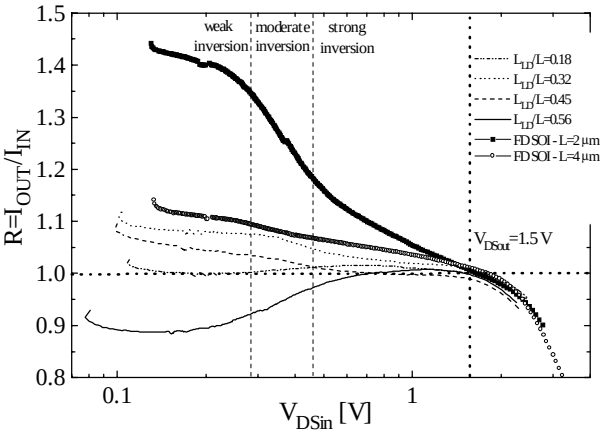

Figure 5. Measured output to input ratio (V_{DSout}=1.5 V) as a function of input transistor drain-to-source potential drop..

All the measured curves are very close to the unity indicating that the presented results are exclusively due to the device structure and are not being affected by the transistor mismatch.

The GC CMs present extremely improved output behavior in all regions of operation, even if compared to the FD CM with L=4 µm. The main advantage of the GC CM against the FD ones is observed in weak and moderate inversion regimes. Generally, current mirrors operate in strong inversion and the advantages of using GC CM are also present in the onset of the strong inversion regime compared to the conventional FD CM.

Figure 6 presents the I_{OUT} (A) and the required V_{DSin} (B) *versus* V_{DSout} curve, extracted with a constant I_{IN} of 100 µA for the W/L=18/2 GC CM with different (L_{LD}/L) and FD CM with W/L=18/2 and 18/4.

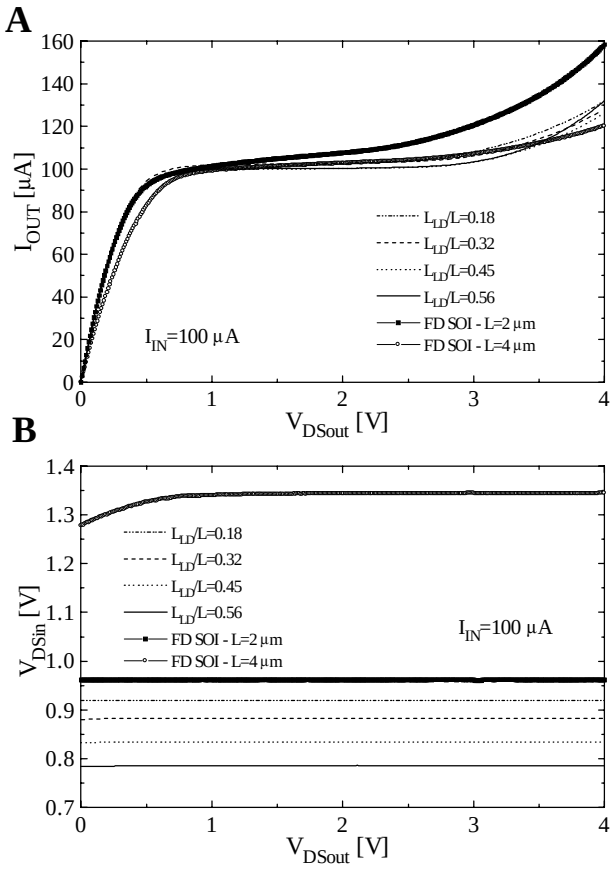

Figure 6. Measured I_{OUT} (A) and the required V_{DSin} (B) against V_{DSout} for a constant I_{IN}=100µA.

The reduced channel length modulation and larger drain breakdown voltage of any GC transistor improves the CM output swing for similar L. A very slight dependence of the output characteristics on the L_{LD}/L ratio has been found, which confirms the minimization of the misalignment problems in the GC CM fabrication. For an output drain bias up to 3 V the

GC CM output characteristics are closer to the FD CM with 4 μm, which points out the possible area reduction provided by GC transistors for similar performance.

In addition, the required V_{DSin} to obtain similar I_{OUT} is smaller in any GC CM than in the FD CM with similar L, due to the effective channel length reduction.

Figure 7 plots I_{OUT} as a function of V_{DSout}, varying the input current from 10 μA to 50 μA (steps of 10 μA) for the GC CM with different (L_{LD}/L) and FD CM, all with W/L=18/2.

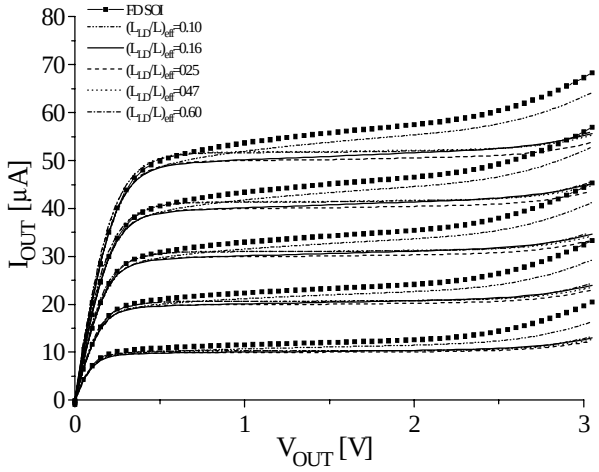

Figure 7. Measured I_{OUT} x V_{DSout} extracted varying the I_{IN} from 10 μA to 50 μA (steps of 10 μA).

Figure 7 confirms the improvement of CM output performance even for reduced input currents. This curve also shows that the GC CM with the lowest L_{LD}/L starts to present a degradation in the output conductance as in conventional transistors which points out an inferior limit to the L_{LD}/L ratio.

3. Self-Heating Measurements

Measurements of the self-heating effect[6-7] were performed on the studied devices according to the technique described in [8-9]. Initially the CM has been biased in saturation but with the output device kept unbiased and connected to a high impedance voltimeter, in order to directly access the source series resistance (R_S). The extracted values for each device were 3.3 Ω, 2.9 Ω, 2.8 Ω and 2.9 Ω for the FD and GC withL_{LD}/L=0.18, 0.32 and 0.45 current mirrors, respectively.

The verification of the self-heating effect is realized by biasing the input transistor with a constant current of I_{IN}=1.5 mA, which causes a V_{DSin} larger than 3 V, and varying V_{DSout} from 0 to 3 V, monitoring V_{DSin} and the current in the shared source (I_S). In this condition both devices are in a region in which the impact ionization is negligible.

In isothermal conditions no modification in V_{DSin} should be verified when changing V_{DSout}. However, if the heating generated in the output device is transferred to the input one, it will reduce the minority carrier mobility and increase the required drain bias to sustain the reference current I_{IN} [8-9].

Figure 8 presents the measured variations of V_{DSin} as a function of V_{DSout}, i.e. ΔV_{DSin} which is difference between the initial V_{DSin} (V_{DSout}=0V) and each measured point, after compensating the potential drop on R_S.

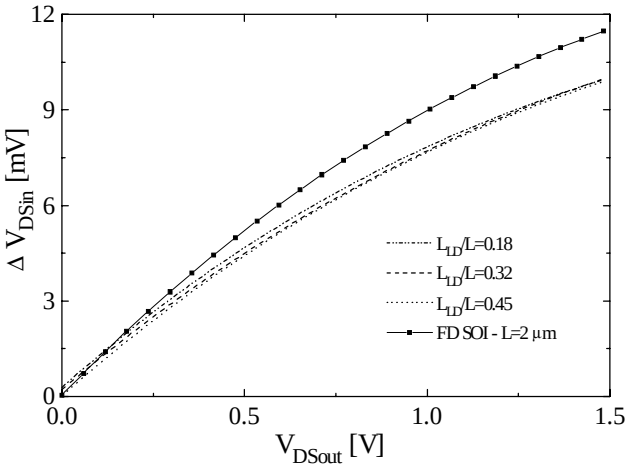

Figure 8. Measured ΔV_{DSin} x V_{DSout} for a constant I_{IN}=1.5 mA.

The results indicate less self-heating occurrence in GC than in FD transistor with similar channel length and output power, so that the presented results are not being influenced by such effect.

4. Conclusion

In this paper we compared the use of conventional and Graded-Channel fully-depleted SOI MOSFETs in current-mirrors. Graded-Channel current mirrors present superior output characteristics in all regions of operation, improving the output swing for the same mask channel length, which makes such device a good candidate for this type of analogue building block. For similar output performance, Graded-Channel current-mirror may reduce the required die area. Only very slightly dependence of the output characteristics on the mask misalignment intrinsic to the Graded-Channel device process has been found. Finally, less occurrence of self-heating effect has been observed.

Acknowledgements

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