A Bandgap Adjustment Strategy for Temperature Centering and Spread Reduction

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Abstract

Circuit random offset, component mismatching and process deviation cause chip-to-chip bandgap voltage variations which can be minimized considering a proper design strategy. Moreover, since simulation results can not usually be considered completely reliable, a tweak strategy to center the bandgap voltage across temperature must be adopted. The design strategy for temperature centering and spread reduction of a low voltage bandgap circuit in a 0.8μm CMOS technology is described here. Applying this method, the standard deviation of the bandgap voltage was reduced to 15mV and the average bandgap voltage variation was less than 14mV for a temperature ranging from -40 to 135 Celsius degrees.

1. Introduction

The design of analog circuits is commonly affected by offset and mismatching of devices. Quite often, process are characterized for digital applications only and limited data is available for matching of components as function of area and size. With the trend for systems-on-a-chip, it is becoming more and more frequent the inclusion of analog blocks together with digital cores and blocks. One can argue that a process should be completely characterized for analog applications as well, but in reality the opposite is true. It has been observed with the use of foundries that, in general, focus is just on characterization for digital designs as it is faster and takes less time and resources.

The analog designers faces then the challenge to design precision analog blocks without fundamental data. Usually, an analog design takes data and results from previous designs and tries to do its best guess on the behavior for a new technology, using the most robust approach for the circuits. After the prototypes are tested, deviations will show up and adjustments need to be done.

One of the most painful problems to be detected and measured is offset resulting from device matching. Measuring a few millivolts on a top of several volts common mode in a closed loop circuit is painful and time consuming. To aggravate the problem, mismatches are random by nature and a large sample of points have to be measured for one to come up with a meaningful conclusion. A methodology to address the most offset sensitive nodes and devices and correlation between measurements and simulations is presented. Using this technique, the number of passes to make an analog block meet specifications is minimized. Moreover, a resistor trimming technique is also presented. This methodology is generic and can be applied to any analog circuit. In this work, a bandgap voltage reference is used to demonstrate its use and results.

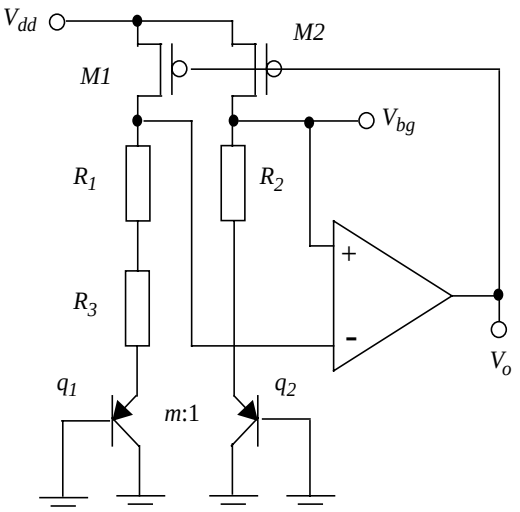

Fig. 1. The bandgap circuit

Bandgap circuits are widely used to generate a stable DC reference voltage ideally insensitive to process and temperature changes. However, such kind of circuits are affected by process variation, devices matching and random offset coming from its building blocks (operational amplifiers, bipolar devices, resistors, etc.). Mismatching problems and random offset sources depend strongly on the specific circuit architecture and must be judged case by case.

The bandgap circuit generates a reference voltage that is independent of temperature by cancelling the negative temperature coefficient of a *pn* junction (or V_{be} for a diode connected bipolar transistor) with the positive temperature coefficient of a PTAT (proportional-to-absolute temperature) circuit. The PTAT is based on the temperature voltage (V_T) scaled by a constant which is made up of circuit parameters. The derivation of the bandgap equations can be found in standard textbooks [1,2]. Referring to the circuit in Fig. 1 with transistors *M1* and *M2* identical, the bandgap voltage is given by:

$$V_{bg} = V_{be} + \frac{R_1}{R_3} \cdot \ln\left(\frac{ae_1}{ae_2} \cdot \frac{R_2}{R_1}\right) \cdot V_T \qquad (1)$$

where V_{bg} is the bandgap voltage, V_{be} is the base-emitter voltage of transistor q_2, and ae is the bipolar emitter area. When the zero temperature coefficient is imposed at $T = T_0$:

$$\left.\frac{\partial V_{bg}}{\partial T}\right|_{T=T_0} = 0 = \left[\frac{\partial V_{be}}{\partial T} + \frac{R_1}{R_3}\cdot \ln\left(\frac{ae_1}{ae_2}\cdot\frac{R_2}{R_1}\right)\cdot\frac{\partial V_T}{\partial T}\right]_{T=T_0} \quad (2)$$

the resistor ratio (R_1/R_3) and the bipolar emitter area ratio ($m = ae_1/ae_2$) can be adjusted properly (assuming $R_2 = R_1$). In spite of the cancelling in (2) at $T = T_0$ being not perfect because ($\delta V_T/\delta T$) varies linearly with temperature whereas ($\delta V_{be}/\delta T$) has a slightly parabolic temperature dependence, it is possible to attain typically a few mV variation in the temperature range. Once again, a poor matching will cause an inappropriately bandgap voltage centering with temperature.

This paper is organized in the following manner. In Section 2 is described a method to evaluate the main random offset sources for a specific bandgap circuit and a technique to reduce their impact on the reference voltage spread. In Section 3 is presented a tweak strategy to center the bandgap vs. temperature curve giving a rapid prototyping tuning. Finally, Section 4 illustrates the experimental results when these design criteria are applied to a bandgap circuit in a 0.8µm CMOS process. The main conclusions are summarized in Section 5.

2. The bandgap spread reduction technique

Since the bandgap must operate from a 5V to 1.8V power supply, it was adopted a low voltage topology for the operational amplifier (see Fig. 2). It is a high gain, two-stage *n*-channel input folded-cascode amplifier able to drive the bandgap circuit with a reduced power supply of 1.6V. Resistor R_F and capacitor C_F are used for lead compensation. Bias network is not shown.

As stated before, random offset and mismatch of an individual circuit have an intrinsic relation with its topology and layout. Using transistor quads based on common-centroid geometry and an unity resistor approach, the layout can be carefully optimized to minimize mismatch. In regard to circuit topology, in bandgap circuits the feedback loop guarantees to keep the amplifier inverting and non-inverting input voltages equal. However, any circuit mismatch will appear at the amplifier input as an offset voltage and translated to the output amplified by the resistor ratio. Therefore, a random offset will cause a bandgap voltage shift different from chip to chip. This fact makes mandatory a plan to reduce the bandgap voltage dispersion.

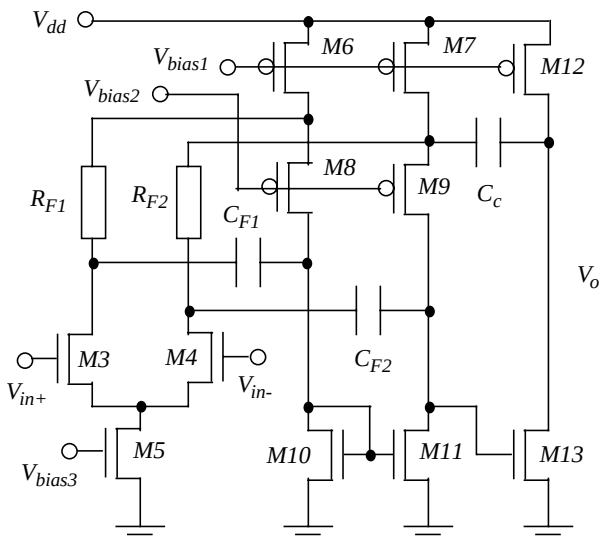

Fig. 2. Low-voltage operational amplifier

As there was none available and/or reliable data on device matching for the target technology as a function of component dimensions/area, it was necessary to determine that combining bandgap experimental data with its simulation results. First, it was estimated via simulation the bandgap voltage sensitivity to the offset sources. Next, based on measurements and statistics of over 100 samples, it was made a regression to establish each offset voltage value that would cause the results observed in real parts.

For the bandgap in Fig. 1 using the operational amplifier in Fig. 2, the random offset sources are the following: (a) mismatching between bandgap inverter drivers *M1-M2*, bandgap resistors R_1-R_2 and resistor ratio R_1/R_3; (b) leakage and/or low emitter current biasing the bipolar transistors q_1 and q_2; (c) matching error at the input pair *M3-M4*, current sources *M6-M7*, cascode devices *M8-M9*, and *n*-channel mirror *M10-M11*.

In order to establish the bandgap sensitivity it was adopted a random offset voltage inherent to a MOS transistor pair as a function of the root square gate transistor area:

$$V_{os} = \frac{K}{\sqrt{a_g}} \quad (3)$$

where V_{os} is the offset voltage, a_g is the gate transistor area and K is a empirical constant depending on physical parameters. Equation (3) is a good fitting of actual behavior, provided MOS transistors W and L are sufficiently larger than minimum size.

Using a hypothetical 1mV offset voltage for pair *M1-M2* and scaling that to the remainder mismatch sources since:

$$V_{os1}\cdot\sqrt{a_{g1}} = V_{os2}\cdot\sqrt{a_{g2}} \quad (4)$$

and also assuming that $K_p=2K_n$, each particular offset impact on the bandgap voltage shift was simulated. Fig. 3 shows the effect of the individual offset related to the total bandgap deviation and Fig. 4 exhibits the accumulated error offset contribution. It is evident a mismatch at the bandgap inverter drivers *M1-M2* has the most severe influence. The offset arising from mismatch between *M1-M2*, current sources *M6-M7* and the *n*-channel mirror *M10-M11* are responsible for 86.5% of the total bandgap voltage error. The resistor ratio mismatch has a little impact on the bandgap deviation (<0.1%) being really important as for temperature centering (see Section 3).

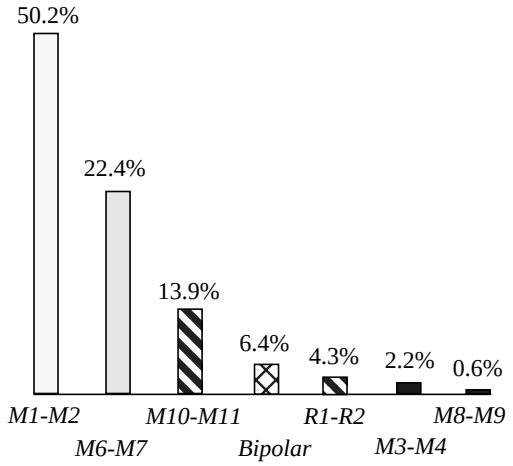

Fig. 3. Contribution of offset sources to bandgap voltage shift

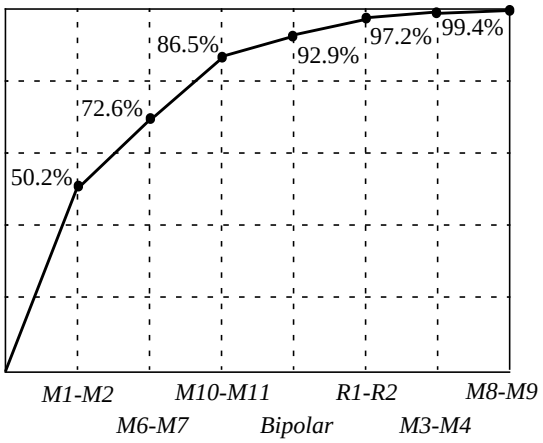

Fig. 4. Normalized Pareto chart of offset contributions

Now, the constants K_p and K_n must be determined and the root square gate area law in (3) validated. Before applying the reduction spread technique, the bandgap reference had a large dispersion of 147mV. Since inverter drivers offset contributes with 50.2% to the total deviation, the partial bandgap voltage shift considering only the *M1-M2* mismatch is ΔV_{bgM1}=0.502x147mV=73.84mV. From (3) and calling the simulated bandgap shift generated by 1mV offset in pair *M1-M2* as ΔV_{bgS1}, the constant K_p is given by:

$$K_p = 73.84\times10^{-3} \cdot \frac{\sqrt{a_{gM1}}}{\Delta V_{bgS1}} \qquad (5)$$

The result in (5) must be fed back in (3) to find the real offset voltages present in the current circuit and, after that, entered as simulation inputs to check the analysis consistency. The total bandgap voltage dispersion obtained from simulation was 148mV in average, including temperature and process variations, which is pretty close to the experimental results mentioned above.

It is important to point out the bandgap specification allowed for 34mV of total dispersion. So, to reduce the reference voltage spread it is imperative to increment the

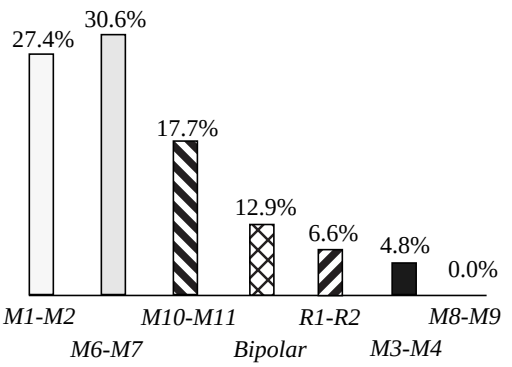

Fig. 5. Bandgap voltage shift owing to offset sources in adjusted circuit

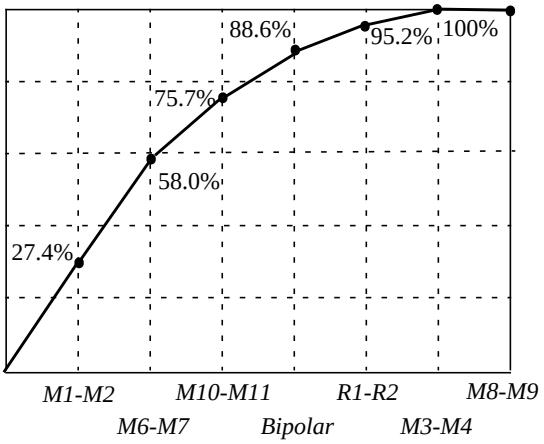

Fig. 6. Pareto chart of adjusted circuit

transistor area and decrease mismatch and offset voltages. As offset in *M1-M2*, *M6-M7* and *M10-M11* are the crucial spread contributors, it seems reasonable to increase their gate areas maintaining a good global trade-off. After some iterations it was found that increasing *M1-M2*, *M6-M7* area 9 times, and *M10-M11* area by a factor of 7 satisfies the specification. Fig. 5 illustrates the individual offset effect on the total bandgap shifting after fixing the key transistor areas. Now, offset coming from mismatch in bipolar transistors and bandgap resistors have approximately 20% of impact on the total deviation. The Pareto chart in Fig. 6 displays the accumulated error contribution of each offset source. It is more smoothly distributed than that in Fig. 4.

Other constraints linked to other specifications usually do not allow to equalize all errors, as would be desired.

The linear sum of each offset contribution is not a realistic approach in calculating the total bandgap voltage dispersion because in real parts all the mismatches will not always be at their maximum value and the offsets will not always have incremental effects, i.e. with same sign. Actually, the offsets will have a combination of positive and negative polarity in a random fashion. A good approach to determine the global offset impact is adopting the root mean square (rms) value of the bandgap voltage given by:

$$\Delta V_{bg} = \sqrt{\Delta V_{bgM1}{}^2 + \Delta V_{bgM6}{}^2 + \ldots} \qquad (6)$$

Taking into account 4 of the major error sources (MOS transistors only) which contribute with 80.5% of the total shifting, the rms bandgap voltage deviation is $\Delta V_{bg85\%}$=27.9mV. As long as the goal is to have a maximum dispersion of 80.5%(34mV)=27.4mV, the solution would be slightly below target.

Considering the remainder sources, bipolar transistors and bandgap resistors, the total rms bandgap voltage deviation is ΔV_{bg}=29.3mV, which meets the specification.

The experimental results after the described method was applied will be discussed in Section 4.

3. The tweak strategy for bandgap voltage temperature centering

Prototype results not always correspond to simulation and some adjustment becomes necessary. In the case of the bandgap circuitry, the curve of voltage across temperature is expected to be an inverted parabola with the peak centered halfway between minimum and maximum temperatures defined in the specification. However, prototypes were out of centering in the first iteration.

For the circuit in Fig. 1, as modifying the emitter area ratio to center the bandgap voltage across temperature is not practical (see expression (2)), a resistor ratio adjustment is needed. A desirable tweak is the one which requires the lowest number of layers to be modified. The goal is to achieve the tweak with only one layer change. Usually the layer chosen for the tweak is the top most metal because it allows partially processed wafers to be waiting for the last few layers to be finished. Another reason to use the upper metal layer is to make the cut of tracks on chip prototypes easier to evaluate the tweak results before ordering a new mask and wafer run.

The adjustment by metal layer, though, implies the insertion or removal of component segments so to adjust the tweakable value. The size of each segment defines what is the resolution for the tweak. A well dimensioned resolution will allow a good final tweak, while under estimated resolutions may return only fairly good results. If the adjustment resides in a critical and also sensitive circuitry the evaluation of tweak based on steps may be a non-trivial task, also risky and time consuming.

In order to allow simpler assessments in the tweak values, prototype data acquisition and continuous adjustment values, an approach that combined prototype measurements and layer modification was adopted.

The bandgap resistors layout is composed by an array of unity resistor interconnected appropriately to obtain the designed values. Additionally, a network made up of unity resistor is placed in both the upper resistors R_1 and R_2, and the lower resistor R_3. The bandgap resistor ratio can be regulated adding extra resistor either at the upper resistors (both R_1 and R_2 equally) or at the lower resistor

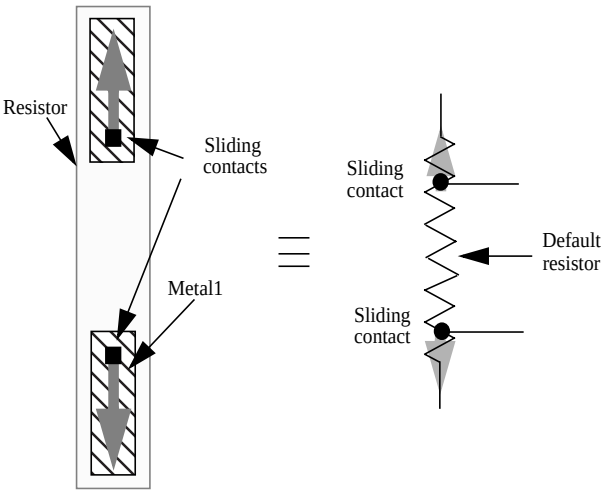

Fig. 7. Bandgap resistor ratio tweak strategy

by cutting metal lines. Although experimental data for the original circuit had shown a monotonically increasing bandgap voltage dependence with temperature, requiring a resistor ratio reduction, it was provided the possibility to increase and decrease this ratio to obtain more flexibility.

The adjustment by upper metal layer was still used, but in a simplified way. A circuitry that allows the increase of bandgap upper or lower resistors by cutting upper metal was added in the layout. In this simplified approach, the evaluation of maximum range of adjustable values is still important to guarantee that the maximum variation would be covered by the proposed adjustment range, but here the resolution was secondary.

Chip prototypes were used for experimental evaluation. By cutting the upper metal tracks the *close to ideal* value was determined. The resolution was less important because the value to be obtained with the prototypes would be for orientation purpose only. The ideal tweak value was expected to be found between two consecutive cut configurations. Once the best configuration was found, the metal adjust circuitry was abandoned as it had shown by interpolation what was the optimum tweak value. The final adjust would actually be done with the contact layer. That layer allows a continuous adjustment, just like the cursor of a potentiometer. So, in order to optimize the prototyping tuning, the bandgap resistors have the possibility to fit the unity resistor value through sliding contacts in both ends of the resistor, as depicted in Fig. 7. If the upper resistor was to be increased in the final layout, contacts in each side of its main bars would slide equally to increase the overall resistance. If the lower resistor was to be increased, the contacts in each side of its main bars would slide equally to increase its resistance value. Then, the symmetry loss at the layout level in the bandgap resistor is minimized. The maximum metal layer extension to slide the contact must be chosen carefully to cover the bandgap voltage dispersion as discussed in Section 2.

A new contact mask was then designed based on the value determined in the experimental procedure, divided equally among all unity resistors to be adjusted. No excessive time to estimate tweak values had to be spent, providing a refinement process less expensive and reducing the turnaround time. On the other hand, an accurate adjustment based on real chip results could be achieved. The trade-off was an additional circuitry only used for prototype evaluation. The critical nature of the bandgap fine adjustment, though, fully justified the approach.

4. Measurements results

In order to verify the circuit optimization techniques described before, a bandgap circuit fabricated using a conventional 0.8μm CMOS technology was adjusted. Table 1 summarizes the bandgap reference circuit performance from the first iteration and the target required to satisfy the specifications. For the bandgap dispersion a 3σ was adopted, where σ is the standard deviation. The available experimental data indicated a monotonically increasing bandgap reference with temperature, i.e. the circuit was not well centered. Temperature ranges from -40 to 135 Celsius degree and the power supply varies from 1.8V to 5V.

Table 1: Prior bandgap performance

Bandgap voltage dispersion 3σ		**Bandgap voltage variation with temperature**	
First iteration	Target	First iteration	Target
147mV	34mV	100mV	10mV

After applying the spread reduction technique with the calculated area changes in the main critical components of the circuit as mentioned in Section 2, the standard deviation of the bandgap voltage was reduced to σ = 15mV in average. A lot of more than 100 samples was characterized at -40^{o}C, 25^{o}C and 135^{o}C. With this improvement the total bandgap dispersion is approximately 45mV, slightly higher than expected. Mismatch arising from the bias network could add offset. However, the present optimization provides a good trade-off between circuit area and performance.

As for the temperature centering, the ideal resistor ratio adjustment was expected to be found between two cut steps and two contact mask were considered to speed up the tuning. In this case, the sample number was of 160 parts.The first metal mask tweak decreased the variation of the bandgap voltage across temperature to 13.2mV whereas for the second one the fluctuation was reduced to 9.3mV. The features of the last pass are summarized in Table 2.

Table 2: Improved bandgap performance

Bandgap voltage dispersion 3σ		**Bandgap voltage variation with temperature**	
Last pass	Target	Last pass	Target
45mV	34mV	less than 10mV	10mV

5. Conclusions

A systematic spread reduction technique and an adjustment strategy for bandgap voltage reference temperature centering has been developed.

After addressing well-known layout techniques to optimize matching (common-centroid geometry layout and unity resistor approach) the spread reduction technique can be straightforward applied to find the main offset sources in a specific circuit but a careful study of its topology should be developed in advance.

The tweak strategy combines simplicity with robustness giving a short turnaround time when evaluating key analog modules.

These techniques were successfully used to optimize a bandgap circuit providing a good trade-off between area and global performance.

Finally, the method described reduces the number of iterations when designing precision analog circuits on technologies not properly characterized for analog designs.

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