BEHAVIOR OF THE GRADED-CHANNEL FULLY-DEPLETED SOI NMOSFET IN SUBTHRESHOLD REGIME

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Abstract

In this paper is presented and discussed the behavior of the Graded-Channel Fully-Depleted Silicon-On-Insulator nMOSFETs (GC SOI nMOSFETs) in subthreshold region. It was observed that there is not any degradation in the subthreshold slope characteristic to the GC SOI nMOSFET in comparison to the Conventional Fully-Depleted SOI nMOSFET regarding the same effective channel length to both transistors. The MEDICI two-dimensional simulator was used to qualify these results.

1. Introduction

In the recent years Silicon-On-Insulator technology has emerged as a key technology for low voltage and low power mixed analog-digital applications and it has been exhausting studied [1].

One of the major advantages of SOI technology use is the quasi-ideal subthreshold behavior leading the inverse subthreshold slope (or only subthreshold slope) close to the theoretical limit of 60 mV/decade at room temperature. This characteristic presents a good solution to the problem of reducing the threshold voltage without increasing the leakage current, which is of special interest for the increasingly grow low voltage and low power market.

Although SOI technology may provide a large set of advantages at the device and circuit level such as reduced junction capacitance and latch-up free structure, the inherent parasitic bipolar effect (PBE) remains as a problem to overcome since it results in hysteresis, instability during dynamic operation, abnormal subthreshold slope and breakdown voltage degradation [2].

Recently a new device has been introduced to minimize the occurrence of PBE, the Graded-Channel SOI nMOSFET. This device is based in an asymmetric-channel configuration (figure 1), presenting an undoped region in the drain side of the channel whereas the threshold voltage ion implantation is performed in the source side. The overall device characteristics present similar threshold voltage than the Conventional fully-depleted SOI nMOSFET.
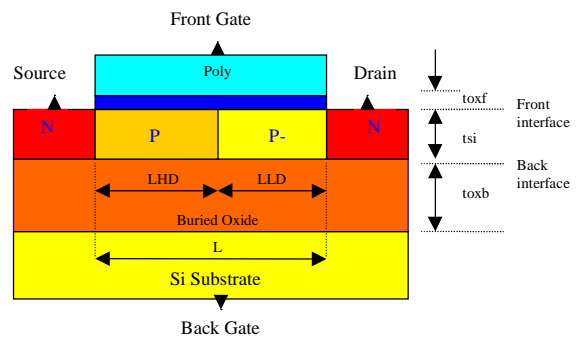

Figure 1: The GC SOI nMOSFET simplified cross section structure. Where t_{oxf}: Front gate thin oxide thickness; t_{si}: silicon film thickness; t_{oxb}: buried oxide thickness; L_{HD}: High doped P region length; L_{LD}: Low doped P region length; L: channel length.

The presented studies show that GC SOI nMOSFET efficiently alleviates the parasitic bipolar junction transistor action improving the breakdown voltage by reducing of impact ionization in the high electric field region. Others advantages of GC SOI nNMOSFET already reported were the extremely flat saturation current presenting almost zero slope and consequently a tremendous reduction in the output conductance increasing the Early voltage (low voltage and low power applications interests) [3-7].

It is known that subthreshold region is particularly important for low voltage and low power applications when MOSFETs are used as a switch in digital logic and memory circuits, because the subthreshold region describes how fast the switch turns on and off [8].

In the reference [4], it has observed that the subthreshold slope characteristic of GC SOI nMOSFET degrades while increasing the length of low doped region which could be a potential problem for circuit applications. This phenomena has not been still scientifically clarified in the current scientific literature. The goal of this paper is to study for the first time, the GC SOI nMOSFET behavior in the subthreshold regime and to compare it with the Conventional SOI nMOSFET.

2. Simulation Results

It is known that in the subthreshold region is defined an important parameter of the MOSFETs, i.e, the subthreshold slope $\{S=\partial V_{GF}/\partial[LOG(I_D)]\}$ [8].
In order to evaluate and study the GC SOI nMOSFET behavior in subthreshold regime, MEDICI two-dimensional simulations [10] were performed with several GC SOI nMOSFET structures, varying the effective channels lengths ($L_{eff}=L_{HD}=L-L_{LD}$) and maintained the channel length ($L=L_{HD}+L_{LD}$) fixed. Physical models for the electric field dependent carrier mobility with velocity saturation, SRH recombination/generation with doping-dependent lifetime, Auger recombination, bandgap narrowing, and impact ionization with electric field were included in the simulations. Simulating these different structures, it was generated several subthreshold slope curves as a function of back-gate bias (V_{GB}), as indicated in the figure 2.
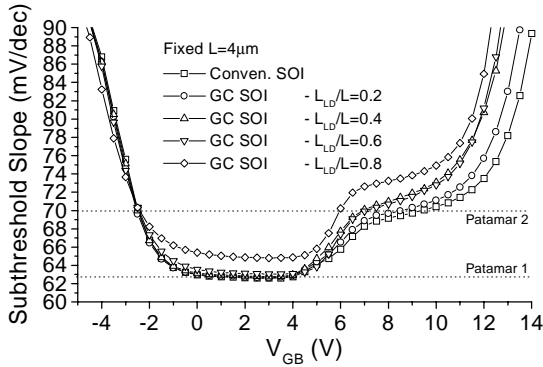

Figure 2: Subthreshold slope curves as a function of V_{GB} to different effective channel lengths ($0.0 \leq L_{LD}/L \leq 0.8$) regarding fixed channel length.

There are two (2) patamars in these curves set. The first one ($S_1 \cong 63mV$) represents the GC SOI nMOSFET current is flowing from drain to source near to the front interface and the second one ($S_2 \cong 70mV$) represents the current is flowing near to the back interface [9]. These curves show that subthreshold slope presents a small increase when the L_{LD}/L ratio increases, i.e. when decreases the effective channel lengths, regarding fixed channel length.
It is important to note that, in first order, there is not

subthreshold slope degradation regarding different L_{LD}/L ratios smaller than 0.60 with fixed channel length, $L=4\mu m$. This can also be observed in figura 3 where it is shown the characteristic of subthreshold slope as a function of effective channel lengths (SxL_{eff}). Then, concerning the subthreshold slope the GC SOI nMOSFETs can normally be used in the place of the Conventional SOI nMOSFETs and consequently it gets all the advantages that the GC SOI nMOSFETs have, in comparison to the Conventional SOI nMOSFETs, as described in previous papers.
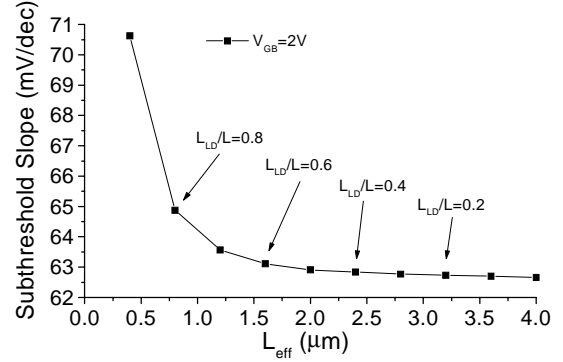

Figure 3: Subthreshold slope (S) as a function effective channels lengths (L_{eff}) with $V_{GB}=2V$.

In order to compare the GC and Conventional SOI nMOSFET behavior in the subthreshold regime with the same effective channel lengths, it has been generated different GC SOI MOSFETs structures with the same effective lengths $L_{eff}=4um$, varying low doped channel lengths (L_{LD}) and consequently the total channel lengths (L). It has been simulated these different structures and generated several subthreshold slope curves as a function of V_{GB}, as indicated in the figure 4.
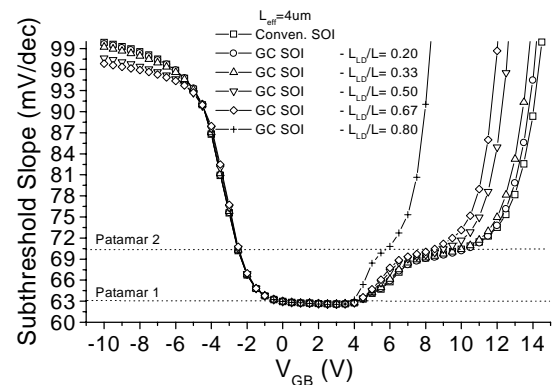

Figure 4: Subthreshold slope as a function of V_{GB} to the same effective channels lengths $L_{eff}=4\mu m$ regarding different channels lengths L.

Figure 4 shows that with the same effective channel lengths, the subthreshold slope of both transistors *are exactly the same in the first patamar region* which

represents the region of the major interest that GC and Conventional SOI nMOSFETs are normally used in mixed analog-digital applications. Thus, the subthreshold slope of the GC SOI nMOSFET is not degraded in comparison to the Conventional SOI nMOSFET regarding the same effective channel lengths. The GC SOI nMOSFET behavior described in the figure 3 is due the effective channel lengths reduction, resulting in the appearing of short channel effects that it degrades the subthreshold slope characteristic in the subthreshold region. This effect is also equality observed in Conventional SOI nMOSFET devices with similar effective channel length.

3. Electrical and Physics Interpretations of GC SOI nMOSFETs behavior in the subthreshold regime

In order to study the electrical and physical behavior of the GC SOI nMOSFET in subthreshold regime, it has been analyzed the potential as a function of the channel depth and a current density lines drawing through MEDICI two-dimensional simulator as follow:

1- Potential: In the figure 5.a and 5.b are shown the potential at $L_{HD}/2$ and at $L_{LD}/2$ respectively, as a function of channel depth to the GC SOI nMOSFET and to the Conventional SOI nMOSFET regarding the same effective channel length and for two different bias conditions of V_{GF} (0.1V-subthreshold region and 0.5V-threshold region). The GC SOI nMOSFET presents the followings physics characteristics: $L=5\mu m$, $L_{HD}=4\mu m$, $L_{LD}=1\mu m$, $N_{HD}=1x10^{17}cm^{-3}$, $N_{LD}=1x10^{15}cm^{-3}$, $t_{oxf}=20nm$, $t_{si}=80nm$, $t_{oxb}=400\mu m$. The Conventional SOI nMOSFET presents the followings physics characteristics: $L=5\mu m$ $N_A=1x10^{17}cm^{-3}$, $t_{oxf}=20nm$, $t_{si}=80nm$, $t_{oxb}=400\mu m$. Both transistors have the same effective channel length, i.e. $L_{eff}=L=4\mu m$ to the Conventional SOI nMOSFET and $L_{eff}=L_{HD}=4\mu m$ to the GC SOI nMOSFET.

In the figure 5, it is observed that the potential in the middle of effective channel length ($L_{eff}/2=L_{HD}/2$) of the GC nMOSFET, and in the middle of effective channel length ($L_{eff}/2=L/2$) of the Conventional SOI nMOSFET *are exactly the same* and consequently the both transistors have the same behavior in subthreshold regime to both bias conditions ($V_{GF}=0.1V$ and $V_{GF}=0.5V$).

It can also observe in the GC SOI nMOSFET that the potential in the low doped channel side (L_{LD}) is different of the potential in the high doped channel side (L_{HD}) because there are two (2) different impurity concentrations in the HD and LD sides. Note also that the L_{LD} side potential along of the front and back interfaces can be considered the same.

As the GC SOI nMOSFET behavior in subthreshold regime is the same of the Conventional SOI nMOSFET regarding the same effective channel length, the

subthreshold slope modeling of the GC SOI nMOSFET is the same of the conventional SOI nMOSFET [9].
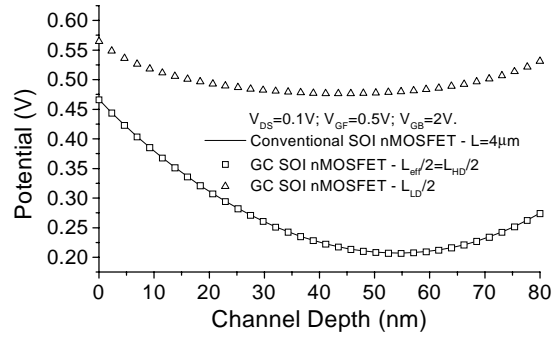
(5.a)
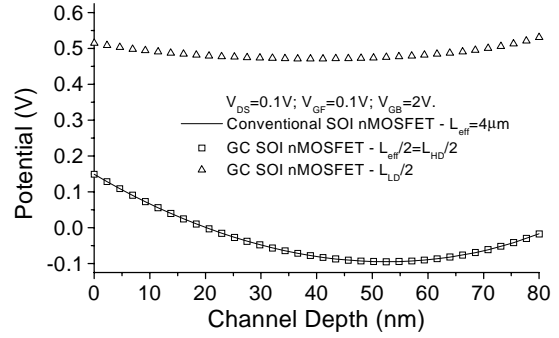
(5.b)

Figure 5: Potential at $L_{HD}/2$ and at $L_{LD}/2$ as a function of the channel depth of the the GC SOI nMOSFET with $L=5\mu m$, $L_{HD}=4\mu m$, $L_{LD}=1\mu m$, $N_{HD}=1x10^{17}cm^{-3}$, $N_{LD}=1x10^{15}cm^{-3}$, $t_{oxf}=20nm$, $t_{si}=80nm$ and $t_{oxb}=400\mu m$ to $V_{GF}=0.1V$ (5.a) and $V_{GF}=0.5V$ (5.b).

2- Current Density Lines: The figure 6 shows the behavior of the current density lines of GC SOI nMOSFET regarding $L=5\mu m$, $L_{HD}=L_{eff}=4\mu m$, $L_{LD}=1\mu m$, $V_{DS}=0.1V$, $V_{GF}=0.1V$ and $V_{GB}=2V$. To this bias using MEDICI two-dimensional simulator, in the HD side, as shown in the figure 5.a, the front interface is weak inverted (0.15V) and the second interface is depleted (-20mV). Thus, the current density lines are bellow of the front interface. It is also observed in the LD side, both interfaces are inverted (both potentials are around 0.52V and they are greater than threshold voltage in this region) and consequently the current density lines are distributed along of the channel depth. It can say that in subthreshold regime, the LD side of the GC SOI nMOSFET behaves like a drain extension.
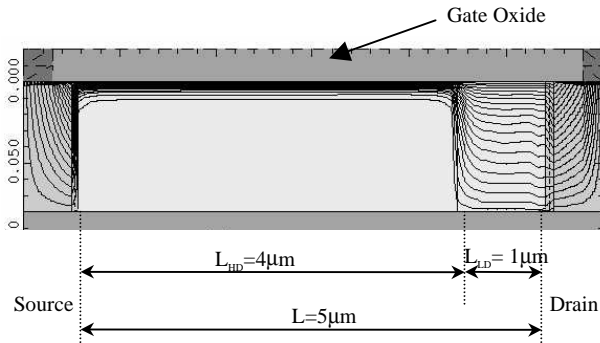
Figure 6: Current density lines drawing of the GC SOI nMOSFET with L=5μm, L_{HD}=4μm, L_{LD}=1μm, V_{DS}=0.1V, V_{GF}=0.1V and V_{GB}=2V.

In the figure 7 is presented the current density at HD side middle (L_{HD}/2) and at LD side middle (L_{LD}/2) respectively, as a function of channel depth. This confirm that in the HD side the current density is bellow of front interface and in the LD side, the current density is distributed along of the channel depth and it has significant values next to the both interfaces. That means, the LD region presents theirs both interfaces inverted and one can say that LD side behaves a drain extension.
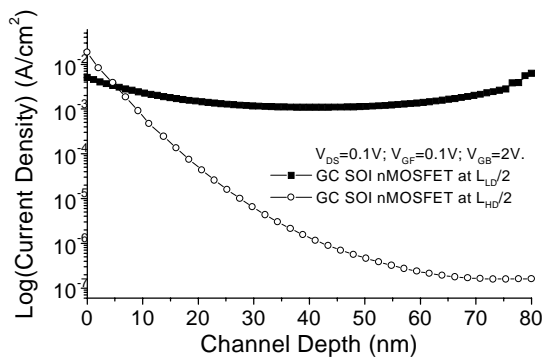

Figure 7: Current density at L_{HD}/2 and at L_{LD}/2 as a function of the channel depth of the the GC SOI nMOSFET with L=5μm, L_{HD}=4μm, L_{LD}=1μm, N_{HD}=1x10^{17}cm^{-3}, N_{LD}=1x10^{15}cm^{-3}, t_{oxf}=20nm, t_{si}=80nm and t_{oxb}=400μm.

4. Conclusions

This paper has studied the GC SOI nMOSFETs in subthreshold regime. It has demonstrated that the GC SOI nMOSFET behavior *is exactly the same* of the Conventional SOI nMOSFET behavior in subthreshold regime regarding the same effective channel length and the subthreshold slope is around 63 mV/decade for both transistors when the front interface is in weak inversion and the back interface is depleted.

There is not subthreshold slope degradation to the GC SOI nMOSFETs regarding different L_{LD}/L ratio smaller than 0.6 to the same physic channel lengths in comparison to Conventional SOI nMOSFET. Thus, it

can be used GC instead Conventional SOI nMOSFET getting all the advantages of the GC SOI nMOSFETs.

It was also observed that the low doped side, region LD, it can be considered like a drain extension in the subthreshold region.

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