A 12-Bit Second Order Sigma-Delta Modulator Design in 0.8μm Low Voltage CMOS

Carlos Renato Trevisan de Mori  trevisan@iee.efei.br
Paulo César Crepaldi  crepaldi@iee.efei.br
Tales Cleber Pimenta  tales@iee.efei.br

Grupo de Microeletrônica – Escola Federal de Engenharia de Itajubá
Av. BFS, 1303 – Itajubá, MG 37500-903 – Brasil

Abstract

This paper examines the design and simulation of a 12-bit Sigma-Delta Modulator that operates from a single 3V power supply. The proposed modulator has been designed with fully-differential switched-capacitor integrators implemented with folded-cascode operational amplifiers. The main goal of the designed modulator is its simplicity. It is shown that is possible to design a precise modulator of moderated Signal-to-Noise Ratio (SNR) using simple circuits, which do not require precise component matching, high precision components or trimming. With an oversampling ratio of 128 and an oversampling frequency of 2.56MHz, the modulator achieves a SNR higher than 74dB (12-bit resolution) for all the simulated cases. The modulator was implemented in a 0.8μm CMOS technology and it measures 560μm x 680μm.

1. Introduction

The low voltage operation is of great importance in portable electronic systems, since it allows a smaller number of batteries, which in turn alleviates the problems of size and weight. In fact, the more systems become portable, the more important becomes the development of basic building blocks in low-voltage. An A/D converter is a very important circuit block that works as an interface between the analog world and the digital signal processing hardware.

In an A/D converter working on low voltage, there is a swing limitation of the input signals, which limits the increase in the Signal-to-Noise Ratio (SNR). A way to maximize the SNR is reducing the noise density in the bandwidth of interest, which is the fundamental property of the ΣΔ modulation.

Due to that property, the ΣΔ modulators (along with the digital low-pass filter and a decimator) have been widely used in A/D converters of high resolution [1,2,3], mainly for the audio frequency range. As another advantage, ΣΔ modulators of moderated SNR are easily implemented and do not require high precision components and neither a precise component matching [4]. Circuits based on ΣΔ modulators are very interesting for design based on standard CMOS processes, since it allows full compatibility of the digital circuit (filter and decimator) and the analog circuit (modulator). The efficiency of such modulators had been demonstrated on a variety of applications [1,2,5,6] such as digital voice processing, instrumentation and telecommunications.

2. Sigma-Delta Modulator

A ΣΔ modulator consists of an analog filter and a coarse quantizer in a closed feedback loop through an D/A converter, as shown in Figure 1. The D/A converter is used to make the digital output signal compatible with the analog input signal. The system is based on the oversampling principle, where the input signal sampling frequency is N times higher (oversampling rate) than the Nyquist frequency (two times the higher signal frequency).

![Figure 1: Block Diagram of a ΣΔ Modulator](image)

The analog filter consists of an integrator. The quantizer, or A/D converter, is just a comparator having only two quantization levels; “1” and “0”. Therefore, it is called coarse quantizer. On the same way, the D/A converter is just a 1bit converter and its output saturates either on the positive reference voltage (+V_ref) or on the negative reference voltage (–V_ref). The block diagram shown on Figure 1 corresponds to a first order modulator. Its order is given by the number of integrators.

From the figure, it can be seen that the difference between the input signal x(t) and the quantized output y(t) is converted back to analog as signal the \(\tilde{x}(t)\). Provided that the D/A converter is perfect and neglecting signal delays, this difference between the input signal \(x(t)\) and the feedback signal \(\tilde{x}(t)\) applied to the integrator input corresponds to the quantization error. This error is summed up in the
integrator and then quantized by the one-bit A/D converter. Although the quantization error at every sampling instance is large due to the coarse nature of the two level quantizer, the action of the $\Sigma\Delta$ modulator loop is to generate a "0" or "1" output, thus producing a Pulse Density Modulation (PDM) at the output.

The quantization process (conversion of an analog signal into a finite range of number system) introduces an error to the quantized signal and it is known as quantization error or quantization noise. The analog filter and the feedback around the modulator shape the large quantization noise produced by the coarse quantizer moving most of its energy to high frequencies. A digital low-pass filter removes this shaped quantization noise so that the signal can be resampled at lower rate to produce the final high resolution Nyquist rate output.

3. Modulator Architecture

The modulator to be designed shall have a 12-bit resolution, that corresponds to a SNR of 74dB. It also must have a frequency up to 10KHz and must operate under a 3V power supply. The second order modulator with an oversampling ratio of 128 is the best architecture for the proposed circuit requirements. It requires less precision and matching components than a third order modulator and can be implemented at lower oversampling rate than a first order modulator. This oversampling ratio corresponds to an oversampling frequency of 2.56MHz at a bandwidth of 10KHz. Figure 2 shows the block diagram of the considered modulator.

Preliminary functional simulations have shown the gains of integrators and D/A converter feedback loops. These gains ensure the nonsaturated integrators output and their stability. The gain for the first integrator (K1) must be 0.25 and 0.5 for the second integrator (K2). The D/A converter feedback gain of the first integrator (d1) is equal to 0.25. For the sake of modulator stability, K1 = 0.75 d2 [5]. Hence, the gain of the second integrator (d2) is equal to 0.375.

Based on the previously defined gains and on the oversampling frequency of 2.56MHz, it was performed a functional simulation of the proposed modulator shown in Figure 2. Figure 3 shows the output signal spectrum for a frequency of 1.25 KHz. The obtained values for SNR, THD and SNDR from the simulation are shown on Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>85.5</td>
</tr>
<tr>
<td>THD</td>
<td>92.3</td>
</tr>
<tr>
<td>SNDR</td>
<td>84.7</td>
</tr>
</tbody>
</table>

Table 1: SNR, THD and SNDR values obtained using Matlab®

As can be observed from Table 1, the SNR value is very close to the expected value of 82 dB previously calculated and well above the theoretically 72dB of SNR required for a 12-bit precision.

Finally, Figure 4 shows the result of several simulations obtained using Matlab® for several sinusoidal input signal amplitudes. The curve on Figure 4 is function of peak input signal normalized by $\Delta V$ ($V_{ref}$). It is important to observe that the SNR is larger as the input voltage is less attenuated when compared to the reference voltage. The largest value of SNR occurs when the input voltage is attenuated by about 3dB when compared to the reference voltage, since the integrators were designed to operate on their high gain regions for this input voltage value.
4. Modulator Design

Figure 5 shows a simplified modulator block diagram. In the fully differential structure shown, the feedback loops are duplicated. Thus, it can be seen two integrators (INT1 and INT2), the comparator, two CMFB circuits (CMFB1 and CMFB2) and four 1-bit D/A converters (D/A1+, D/A1-, D/A2+ and D/A2-).

4.1. Integrators

The integrators will be implemented using the switched capacitor (SC) technique since it allows the simulation of high value resistors without using large area. Nevertheless, this technique suffers from charge injection. The charge injection problem can be minimized by using a full-differential structure. This structure improves the PSSR modulator performance when compared to the single-ended structure. It also doubles the output signal swing which improves the SNR. Additionally, the differential circuit symmetry improves the THD modulator performance because the even order distortion components are canceled, independent of their origin. Nevertheless, the use of the differential structure increases the area. Figure 6 shows the simplified switched capacitor integrator.

Figure 6 also shows the clocking scheme used in the circuit. It uses a basic two-phase nonoverlapping clock (φ₁ and φ₂), along with the delayed additional clocks φ₁D and φ₂D. This arrangement and the differential architecture causes the parasitic capacitances to have the least effect on the circuit operation and the charge injection cancellation. Basically, the charge injection causes a dc offset error and not a harmonic distortion.

The first integrator is the most critical block in the modulator design. Due to the noise shaping, the second integrator can have less restricted specifications. Even though, in order to facilitate the layout, both integrators will have the same specifications defined by first integrator.

Theoretically, the gain of the operational can be the same as the over-sampling rate (128), or 42dB. Unfortunately, a low gain may cause harmonic distortion at the modulator output. It can be avoided by having a gain between 55dB and 60dB. Such order of gain can be accomplished using a single stage amplifier, thus simplifying the design. Therefore, to implement the amplifier, the folded-cascode topology was chosen, which has a high gain when compared to other single stage topologies. This topology is also very popular on a 3V operation due to simplicity, symmetry, high speed and better PSRR when compared to two stage circuits [7]. Figure 7 shows the folded-cascode amplifier.
The minimum value for the sampling capacitors on the integrators have been obtained using equations of SNR degradation in terms of input power signal, thermal noise power and quantization noise power [1,3]. Using these relationships, the value found for $C_i$ must be larger than 27fF for a SNR higher than 74dB. Since the differential structure will be used, the capacitors on both branches of the amplifier must be matched. The value of 27fF is too small for an adequate matching and therefore the value of 0.2pF will be used. For this new capacitor value, the SNR becomes 82dB. An input capacitor ($C_{in}$) equal to 0.2pF yields an integration capacitor ($C_f$) equal to 0.8pF for the first integrator and 0.4pF for the second integrator, according to the previously defined gains.

A bias circuit provides the input bias $P_1, P_2 e N_2$. These bias should be enough to generate a bias current $I_{SS}$ around 25µA to reach the slew-rate requirements. The Common-Mode Feedback Circuit (CMFB) provides the CMFB port.

The Table 2 summarizes the obtained results. The gain requirements previously defined were overcome. The phase margin and unity frequency gain guarantee the satisfactory op-amps operation.

<table>
<thead>
<tr>
<th></th>
<th>Typical</th>
<th>Worst Power</th>
<th>Worst Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain $A_0$ [dB]</td>
<td>71.26</td>
<td>67.69</td>
<td>70.82</td>
</tr>
<tr>
<td>PM [degrees]</td>
<td>82.84</td>
<td>84.46</td>
<td>83.32</td>
</tr>
<tr>
<td>$F_T$ [MHz]</td>
<td>15.15</td>
<td>15.51</td>
<td>10.66</td>
</tr>
</tbody>
</table>

Table 2: Obtained Results with Folded-Cascode Amplifier

The fully differential amplifier requires an auxiliary circuit to define its common-mode output voltage ($V_{OCM}$). This circuit (CMFB) is shown in Figure 8 and it senses “out+” and “out-” outputs and a feedback loop is used to provide the correct common-mode voltage at CMFB port. The CMFB circuit compares $V_{OCM}$ with a reference voltage and establish the correct bias voltage. During the integrator sampling phase ($\phi_1$), capacitors $C_{1+}$ and $C_{1-}$ adjust the reference voltages on $C_{2+}$ and $C_{2-}$. During the integration phase ($\phi_2$), capacitors $C_{1+}$ and $C_{1-}$ are recharged with $V_{OCM}$ and $V_{N1Q}$.

### 4.2. Comparator

The purpose of the comparator in a $\Sigma\Delta$ modulator is to quantize a signal in the loop (1-bit quantizer) and provide the modulator output in a pulse density waveform. Since the comparator appears after the loop gain block and before the output terminal, it is very insensitive to offset and hysteresis. These nonidealities are shaped by the loop in the same way that the quantization noise it produces is shaped.

A circuit topology that reaches all the comparator specifications is shown in Figure 9 [8]. This circuit occupies a small area, it is very fast and low hysteresis. After the comparison, output inverters (not shown in the figure) saturate in VDD or GND level and a SR latch holds the result until the next comparison phase.

### 4.3. D/A Converter

The purpose of the feedback D/A converter (DAC) on the loop of the modulator is to convert the digital output signal back into an analog form to be compared to its analog input signal. Therefore, the performance of the modulator is completely dependent on the accuracy of its feedback DAC and the way in
which its output is compared to the analog input. The DAC is composed by switches, capacitors and a reference voltage which will be used as a reference by the comparator. Depending on the modulator output, the D/A converter will saturate to \( +V_{\text{ref}} \) or \( -V_{\text{ref}} \). The reference voltage is external to the circuit.

Linearity is the main requirement on the DAC. For this reason, the 1-bit DACs are widely used due to its natural linearity. Since they only have two levels, these DACs are guaranteed to be free from differential nonlinearity (DNL), since all step sizes are identical (there is only one step).

The difference between the reference voltage and the sampled input voltage can be implemented in two ways: using the same input voltage branch, i.e., the same capacitor \( C_{\text{in}} \), or using an independent branch, i.e., using another capacitor, named \( C_{\text{d}} \). The second approach increases the thermal noise due to capacitor \( C_{\text{d}} \). This is not a problem since the original capacitor has been increased to 0.2pF to improve the matching. This increase already attends the requirement of increasing the input capacitor to achieve the desired SNR. Therefore, the option was made on independent branches (including \( C_{\text{d}} \)), that also has the advantage of no distortion from the incomplete setting of \( C_{\text{d}} \), since its charge is not dependent on the input voltage. According to the previously defined gains, the capacitor \( C_{\text{d}} \) for the first integrator is equal to 0.2pF and for the second integrator is equal to 0.15pF.

Figure 10 shows used DAC. This circuit guarantees that the reference always sees the same load, independent of transition density, since both capacitors (CIF1 and CIF2) are charged between the reference (REF) and the analog ground (GNDANA) every clock cycle.

![Figure 10: One-Bit D/A Converter](image)

5. Simulation Results

Figure 11 shows the frequency spectrum for an input sinusoidal signal of 2.5KHz for the typical case. It is important to note the noise shaping property of \( \Sigma \Delta \) modulators. From the figure, it can be seen that the modulator attenuates noise at low frequencies and increase it at higher frequencies. The spectrum of Figure 11 was obtained by functional simulations at Item 3.

![Figure 11: Output Modulator Spectrum for the Typical Case](image)

Table 3 summarizes the initially calculated values to SNR, SNDR and THD and these values obtained from modulator electrical simulation for all the cases. The initially proposed SNR was 72dB; however, during the modulator design, the sampling capacitor was increased to 0.2pF. To this more adequate value for the sampling capacitor the calculated SNR should be 82dB. This value is very close to that obtained from simulations, equal to 82.5dB for the typical case. The SNR is quite different to the other cases, but higher than specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Calculated [dB]</th>
<th>Simulated [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>85,5</td>
<td>82,5</td>
</tr>
<tr>
<td>THD</td>
<td>92,3</td>
<td>85,5</td>
</tr>
<tr>
<td>SNDR</td>
<td>84,7</td>
<td>81,4</td>
</tr>
</tbody>
</table>

Table 3: Comparison Between Calculated and Simulated Parameters

The \( \Sigma \Delta \) modulator layout without pads is shown in Figure 12. The circuit was designed on a CMOS AMS 0.8\( \mu \text{m} \) n-well process with two layers of polysilicon and two layers of metal and it measures 560\( \mu \text{m} \) x 680\( \mu \text{m} \). Figure 12 shows the widely used modulator floorplanning [9]. Its main characteristic is to place the analog circuit far away of the digital circuit and the switches (noise sources). Thus, it provides a distribution of the components in such a way that there is no crossing between analog polarization lines and digital bus.
In the figure, the analog devices are placed in the layout center and they are surrounded by capacitors, switches, digital bus and the clock phase circuit.

6. Conclusions

The initial purpose of this work was to design a 12-bit resolution $\Sigma \Delta$ modulator (74dB of SNR) with an input signal bandwidth of 10KHz. Table 3 summarizes the final simulated results achieved with the designed modulator and it shows that these results were higher than the 74dB of specified SNR for all cases. Therefore, a $\Sigma \Delta$ modulator of moderated SNR and oversampling ratio can be implemented using simple circuits without losses to modulator stability and neither severe requirements to analog circuits precision.

Acknowledgment

The authors would like to thank CAPES Foundation for its financial support.

References


