CMOS Integrate and Fire Neuron for Temporal Logarithmic Encoding

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***Abstract*—It is presented the design of an integrate and fire neuron which produces action potentials in times that are related to the logarithm of an input reference current. The circuit is aimed to the implementation of a system based on the model provided by J. Hopfield for the pattern-recognition computation using action potential timing for stimulus representation [1]. The circuit is based on a 0.35 μm CMOS technology and consumes 330 μW. This consumption corresponds to input currents ranging from 10 μA to 90 μA encoded in phase differences between 140 μs and 375 μs.**

I. Introduction

The prodigious capability of biological nervous systems has motivated the development of artificial models of neurons. These models can be made at different levels of abstraction. For example the artificial neural networks are based on simplified models of neurons which produce a continuous output representing a sigmoidal function of the overall input. We can also find conductance based models of neurons implemented in VLSI [2].

Unlike a conductance based neuron, an integrate and fire circuit represents separately the potential prior to the axonal trigger zone and the action potential [3]. In this work it is presented the design of a CMOS integrate and fire neuron aimed to the implementation of the model proposed by Hopfield in [1]. In that model the information is represented by the timing of action potentials. The relative phase of these spikes with respect to a reference sub-threshold oscillation is a logarithmic function of the input to be represented. For a VLSI implementation of this model it is necessary a circuit that codifies an input signal in spikes with such a logarithmic timing. The circuit presented here reproduces that codification. Differently from a previous work [4] in this case an integrate an fire neuron is presented. In the next section it is reviewed the Hopfield model, then in section 3 the integrated and fire neuron is described. In section 4 the results are summarized and finally in section 5 the conclusions of this work are presented.

II. The Hopfield Model

The model proposed by Hopfield, can be viewed as a possible explanation on the way the human brain resolves the analogue match problem [1]. This problem consists in determine if a set of analogue inputs are in a determined proportion. The system shown in figure 1 is based in the proposal of Hopfield. It resolves the analogue match problem as explained here.

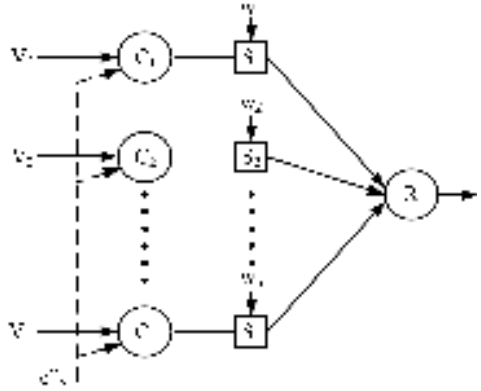

Figure 1. System based on Hopfield model

The system receives a set of analogue inputs $(V_1, V_2, ..., V_n)$ and must detect if it satisfies the equation 1.

$$\frac{V_1}{p_1} = \frac{V_2}{p_2} = ... = \frac{V_n}{p_n} = k \tag{1}$$

Encoding neurons (C_i) generate a train of pulses delayed with respect to a reference signal (clk). This delay (ϕ_i) is a logarithmic function of the respective input (V_i).

$$\phi_i = ln(V_i) + B \tag{2}$$

Delay elements (S_i) adds other delays (δ_i) defined by parameters (w_i). These delays have the relation:

$$\delta_i = ln(\frac{1}{p_i}) + C \tag{3}$$

Then the overall delay after S_i is:

$$\lambda_i = \phi_i + \delta_i = ln(\frac{V_i}{p_i}) + D \tag{4}$$

If the input set satisfies the equation 1 all the delays λ_i would be equals, so a coincidence detector R would generate

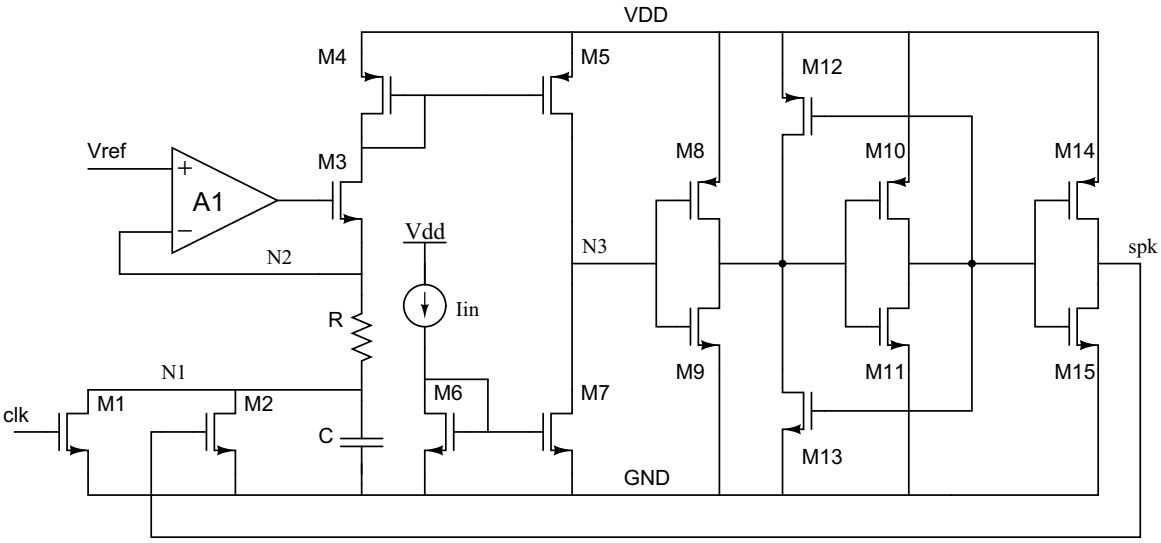

Figure 2. Encoding Neuron

a pulse indicating that the proportion is satisfied.

III. CMOS Integrate and Fire Neuron

The circuit is represented in the figure 2. It consists of an exponential current generator and a schmitt trigger circuit. The exponential current generator is based on an RC circuit. In figure 2 $R, C, M3, A1, M4$ and $M5$ form the exponential current generator, and $M8, M9, M10, M11, M12$ and $M13$ form the schmitt trigger circuit which does the same function as in [5]. The circuit formed by $M5$ and $M7$ acts as a current comparator. When the saturation current of $M5$ is greater than that of $M7$ the voltage at $N3$ is near Vdd, otherwise it is near gnd.

Transistor $M1$ discharges capacitor C to ground periodically. The voltage at node $N1$ rises exponentially toward $Vref$ with a time constant of $\tau = R.C$.

$$V_{N1} = V_{ref}.(1 - e^{-\frac{t}{\tau}}) \tag{5}$$

Current through R falls from $\frac{Vref}{R}$ exponentially to 0. This process restarts every time clk discharges C, so through $M4$ and $M5$ we have a current which varies periodically and exponentially inside each period. That current is compared with the input current Iin at node $N3$.

$$I_{exp} = \frac{V_{ref}}{R}.e^{-\frac{t}{\tau}} \tag{6}$$

While the exponential current is greater than the input one, voltage at node $N3$ is high and voltage at node spk is low. In this case $M2$ is open. When the exponential current is lower than Iin voltage at node $N3$ goes down and spk goes up opening $M2$, then C is discharged, the exponential current returns to its maximal value and $N3$ goes up again. In this way a pulse, interpreted as action potential, is generated at the output node, spk, whenever the exponential current equals Iin. As the current is exponential with respect the time, the time of the pulse generation is a logarithmic function of Iin.

$$t_{spk} = -\tau.ln(\frac{R}{V_{ref}}.I_{in}) \tag{7}$$

For two different inputs I_1 and I_2 we have:

$$t_1 - t_2 = -\tau.ln(\frac{R}{V_{ref}}\frac{I_1}{I_2}) \tag{8}$$

So the relation between to input currents is translated to a difference between the phases of the respective output spikes.

For the calculus of transistors dimensions it was used the Advanced Compact Model of Mosfet [6]. Especial care must be take in the calculus of $M3$ dimensions. When the current of resistor is at its maximum value the voltage at the gate of $M3$ also is at its maximum. As the current is maximal the voltage at the gate of $M4$ is minimal, then it is possible that $M3$ enters in triode region of operation. In order to avoid this condition the following procedure was used. For a good copy of the current the current mirror $M4 - M5$ must operate in strong inversion even at the minimum current. According to [6] strong inversion operation is guaranteed if the normalized current of the transistor is greater than 100:

$$if_4 = if_5 > 100 \tag{9}$$

With the aid of the equation 10 it is possible to calculate the aspect ratios of $M4$ and $M5$.

$$if = \frac{I_D}{ISQ.\frac{W}{L}} \tag{10}$$

In the equation 10 ISQ is a technological parameter. Replacing $if = 100$, $I_D = 5\mu A$ and $ISQ_{PMOS} = 25nA$ we obtain:

$$(\frac{W}{L})_4 = (\frac{W}{L})_5 = 2 \quad (11)$$

Knowing this aspect ratio it is possible to calculate the minimum value of the gate voltage of $M4$. First we calculate the normalized current for the case of maximum current:

$$if_{4max} = \frac{100\mu A}{25nA.2} = 2000 \quad (12)$$

Then the minimum value for the gate voltage is calculated with the aid of the following equation:

$$V_P - V_S = \phi_T.(\sqrt{1+if} - 2 + ln(\sqrt{1+if} - 1)) \quad (13)$$

Where ϕ_T is the thermal voltage and V_P is the pinch-off voltage. We obtain the minimum gate voltage of $M4$ equal to $1.3V$. It means that the saturation voltage of $M3$ must be lower than $1.3V - 1V = 300mV$, where $V_{ref} = 1v$. With this restriction and with the aid of equation 14:

$$V_{Dsat} = \phi_T.(\sqrt{1+if} + 3) \quad (14)$$

we obtain $if_3 = 80$ and then using equation 10:

$$(\frac{W}{L})_3 = 125 \quad (15)$$

Results validating this calculus are presented at the end of the next section in figure 7.

IV. Results

For a time constant of $100\mu s$ values of $R = 10k$ and $C = 10n$ were chosen. In this version an external capacitor is considered. With a clk of $2.5k$ the exponential current varies from $100\mu A$ to $5\mu A$, the frequency of the clk can be increased but the input current range would be reduced.

In figure 3(b) it is represented the pulse generated when a $15\mu A$ input current is applied. The reference clk is presented in 3(a) and the exponential current is shown in 4(a). The output of the current comparator, namely $N3$ is presented in 4(b).

For input currents lower than $15\mu A$ no spike is generated. As the input current increases, the number of spikes inside each clock period increases. In the figure 5 it is presented the curve relating the delays of spikes with the input current. To prove the logarithmic dependence, the exponential of those delays is calculated and the plot is presented in figure 6.

As shown in figure 6 the logarithmic encoding is better than the previous one reported in [4]. The input current ranges from $10\mu A$ to $90\mu A$ corresponding to a spike delays from $140\mu s$ to $375\mu s$.

We made worst case analysis of the circuit. The results in the typical, worst speed and worst power cases are almost the same, this is due to the current mode operation unlike the voltage mode presented in [4].

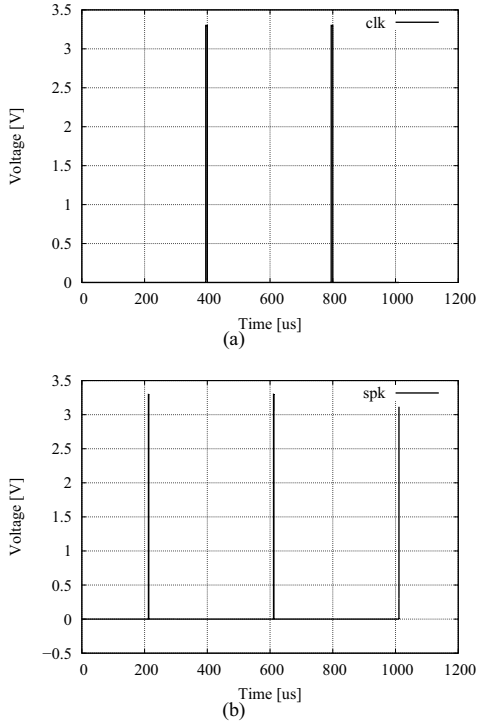

Figure 3. clk and spk for an 15 uA input current

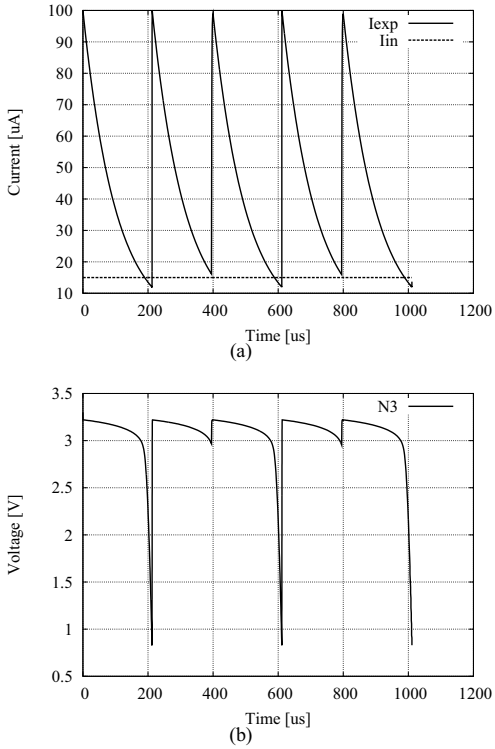

Figure 4. Circuit response for a 15 uA input current

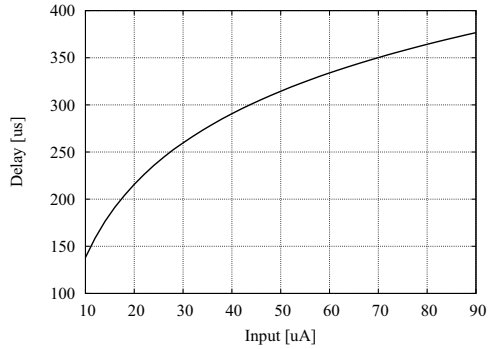

Figure 5. Delays of spikes vs. input current

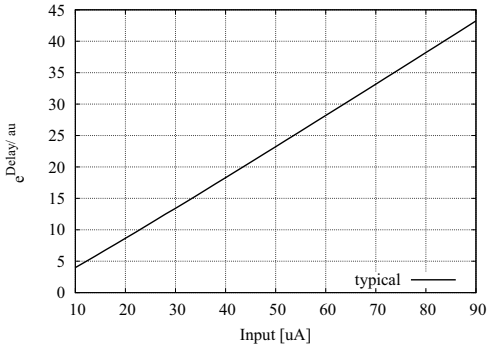

Figure 6. Exponential of the delays

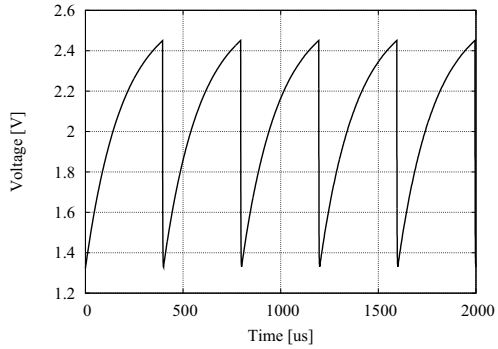

Figure 7. Voltage at the gate of M4

V. Conclusion

It was presented the design of a circuit that encodes input currents into phase delays of outputs spikes. This circuit represents an improved version of that presented in [4].
The input can range from $10\mu A$ to $90\mu A$ and the output delays varies from $140\mu s$ to $375\mu s$ and consumes $330\mu W$. For the design the ACM Mosfet model was used. Simulations was made with the Cadence Spectre simulator. For that case of complex parametric analysis it was used the Cadence OCEAN tool, where OCEAN stands for Open Command Environment for Analysis and allows the development of simulations scripts that simplifies the task of design and characterization. The technology chosen for fabrication was AMS $0.35\mu m$. Future works include a low power version of the integrate and fire neuron presented here like that reported in [7], and the implementation of the system that resolves the analogue match problem described in the section 1. A controlled refractory period can also be included by placing an additional block between the output spike and the transistor that discharges the capacitor. The integration of the time constant $R.C = 10\mu s$ is a problem to be solved in a future work.

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