MCM & LTCC TECHNOLOGY FOR MICROELECTRONICS

TEC-ENC 13

PRESENTATION OUTLINE :

1. MCM Technology
2. Introduction to LTCC Technology
   - **Ceramic Interconnections**
   - **What is LTCC**
   - **Technology Advantages**
   - **Material Systems**
     - **Ceramics, Pastes & Photo-materials**
3. LTCC Processing
   - **Processing steps**
   - **Tape Machining**
     - **Punching, CNC, Laser & JVE**
   - **Lamination**
   - **Sintering**
   - **Bonding to other materials**
   - **Sagging Problem**
3. Photo Patterned Processes
   - **Photo Definable Thick Films**
   - **Photo Sensitive Thick films**
   - **Fodel Compositions**
   - **Diffusion Patterning**
4. New LTCC Systems
   - **Zero Shrinkage Tapes**
   - **LTCC on Metal**
   - **Transfer Tape**
   - **PI-LTCC**
5. LTCC Design Rules
   - **Conductors**
   - **Vias**
   - **Thermal vias**
   - **Capacitors & Inductors**
   - **Printed resistors**
   - **Cavities / Windows**

WHAT IS MULTI CHIP MODULES (MCM)

- A Multi Chip Modules, abbreviated “MCM”, is described as a package combining multiple ICs into a single system-level unit.
- The resulting module is capable of handling an entire function. An MCM can in many ways be looked upon as a single component containing several components connected to do some function.
  - **The components are normally mounted un-encapsulated on a substrate where the bare dies are connected to the surface by wire bonding, tape bonding or flip-chip. The module is then personated by some kind of plastic moulding.**
  - **The module is then mounted on the PCB in the same way as any other QFP or BGA component.**

MCM ADVANTAGES

- MCMs offer an astounding variety of advantages instead of mounting packaged components directly on the PCB:
  - **Performance improvements, such as shorter interconnect lengths between die (resulting in reduced timem of flight), lower power supply inductance, lower capacitance loading, less cross talk, and lower off-chip driver power**
  - **Miniaturization, since MCMs result in a smaller overall package when compared to packaged components performing the same function, hence resulting I/O to the system board is significantly reduced**
  - **Time-to-market, making them attractive alternatives to ASICs, especially for products with short life cycles**
  - **Low-cost silicon sweep, allowing integration of mixed semiconductor technology, such as SiGe or GaAs**
  - **Configuration as hybrids, including surface mount devices in the form of chip scale or micro-ball grid array (BGA) packages and discrete chip capacitors and resistors**

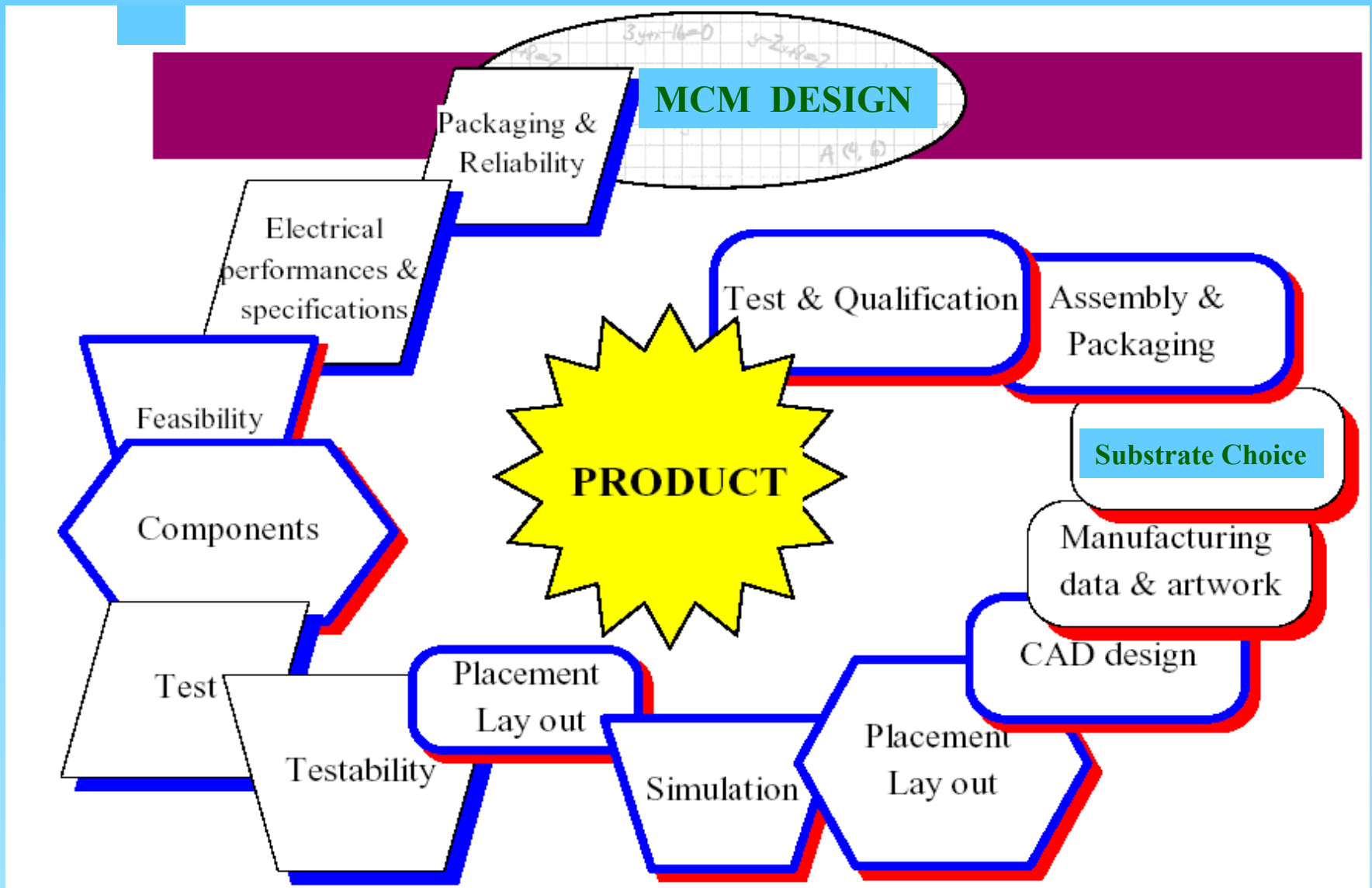
MCM ADVANTAGES

- Simplification of board complexity by sweeping several devices onto one package, thereby by reducing total opportunities for error at the board assembly level, as well as allowing for a cheaper PCB
- Improved reliability by decreasing the number of interconnects between “components” and boards
- Adding new functions to a fixed footprint
- Capability of accommodating a variety of second-level interconnects. While BGA are the most popular, lead-frame solutions can be employed for plugability, enabling modularity for upgrades.

MCM DISADVANTAGES

- Although there is many good reasons for using MCMs, there are also some difficulties and disadvantages.
  - **The most important problem that hinders a more widespread use is the availability of components in "Bare Die" form. Although the market is improving, there is still a long way to go before most components areavailable as "Bare Dies".**
  - **The other concern is cost. Although the newer MCM-L technologies have a low cost potential, cost is rarely the sole reason for going into MCMs.**

MCM DESIGN


MCM DESIGN
Packaging & Reliability
Electrical performances & specifications
Feasibility
Components
Test
Testability
Placement Lay out
Simulation
Placement Lay out
CAD design
Manufacturing data & artwork
Substrate Choice
Assembly & Packaging
Test & Qualification
PRODUCT

MCM TECHNOLOGIES

	TkF	PCB	Dyco	ThF	HTCC	LTCC	DP	GUN
Line width	200	150	80	50	250	250	200	100
Line to line distance	200	150	80	50	150	250	200	100
Diameter	400	500	80	50	200	200	250	100
Integrated resistors	yes	no	no	yes	no	yes	yes	yes
Buried resistors	no	no	no	no	no	tbd	no	yes
Buried capacitors	limited	no	no	no	no	tbd	no	yes
Number of layers	6	12	4	5	>20	>20	4	6-12
Thermal coefficient of expansion (ppm/°C)	6.8	17	20	6.8	6.8	5.8	6.8	4
Thermal conductivity (W/m °C)	24	0.2	0.2	>20	>20	2-6	24	high
Integrated packaging	no	no	no	no	yes	yes	no	limited
Dielectric constant	9	4.6	4	9	9	4.7	9	4
Electrical conductivity (metallization)	+	+	+	+	-	+	+	high
Direct die attach	+	-	-	+	+	+	+	+

Legend

TkF:	Thick film	HTCC:	High temperature cofirable ceramics
PCB:	Printed circuit board	LTCC:	Low temperature cofirable ceramics
Dyco:	Dycostrate®	DP:	Diffusion pattern
ThF:	Thin film	GUN:	General user needs

MCM SUBSTRATE COMPARISON

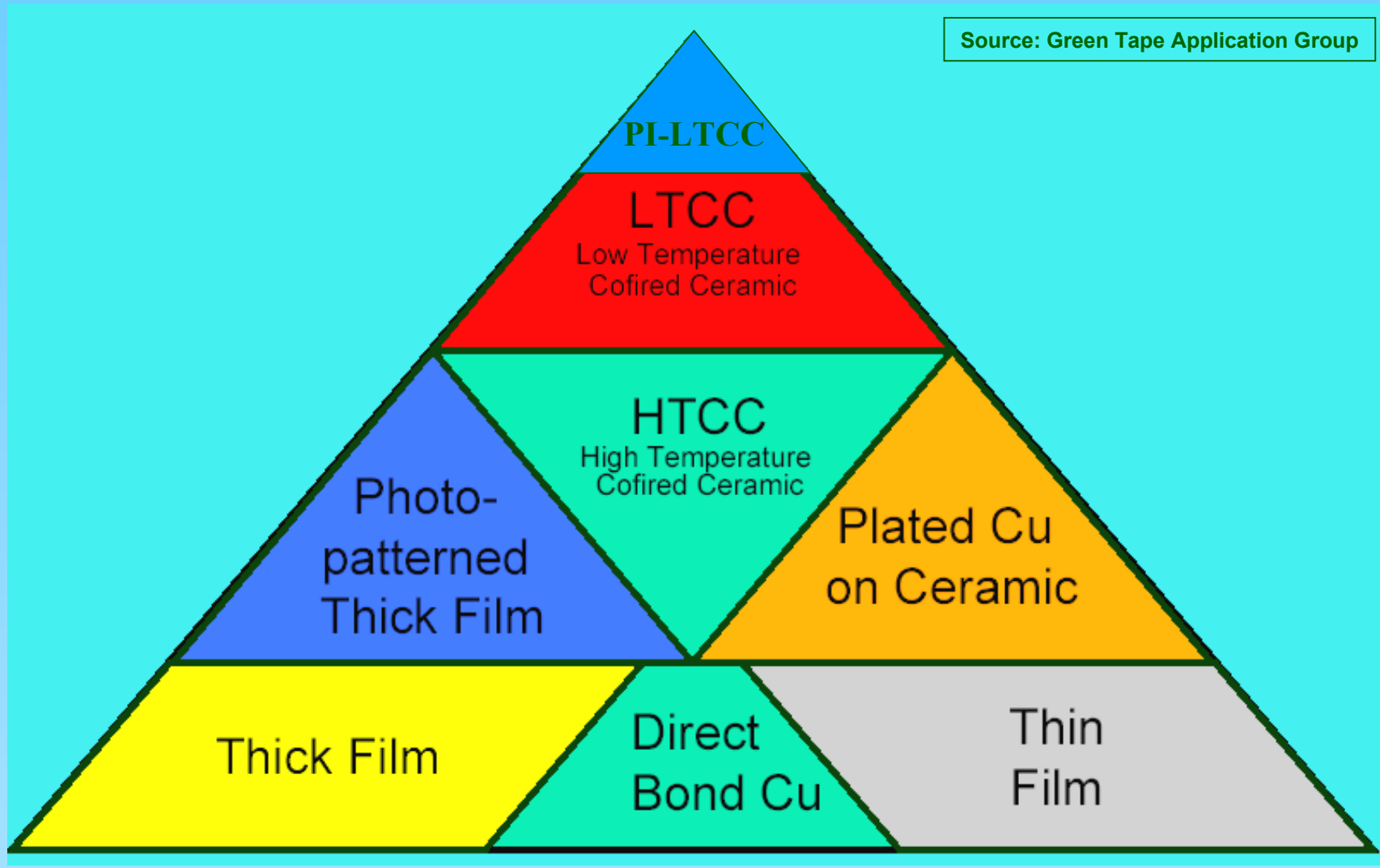
	Ceramic		Organic		
	LTCC	HTCC	FR-4	Advanced	PTFE
Electrical performance	++	+	-	-	++
Integral passives and functions	++	-	-	+	-
3-D structures	++	-	-	-	-
Interconnect density	+	+	-	-	-
Resistors	+	+	-	-	-
Thermal performance	+	++	-	-	-
Board/substrate size	-	-	++	+	+
Microelectronic process	+	+	-	-	-
Reliability	++	++	+	+	+

++ indicates signifigant advantage

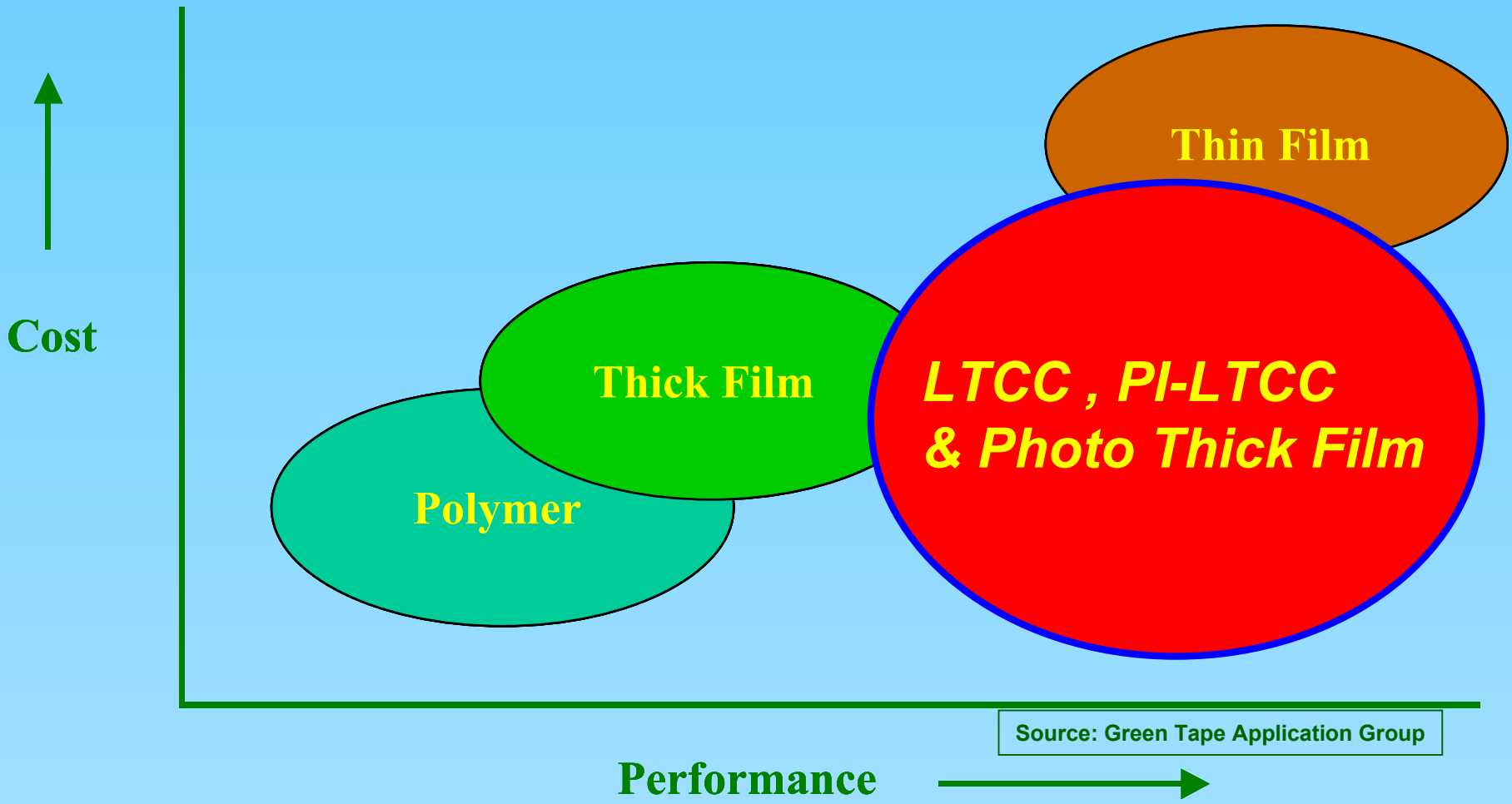
INTRODUCTION TO LTCC TECHNOLOGY

- Ceramic Interconnections
- What is LTCC
- Technology Advantages
- Material Systems
  - Ceramics
  - Pastes
  - Photo-materials

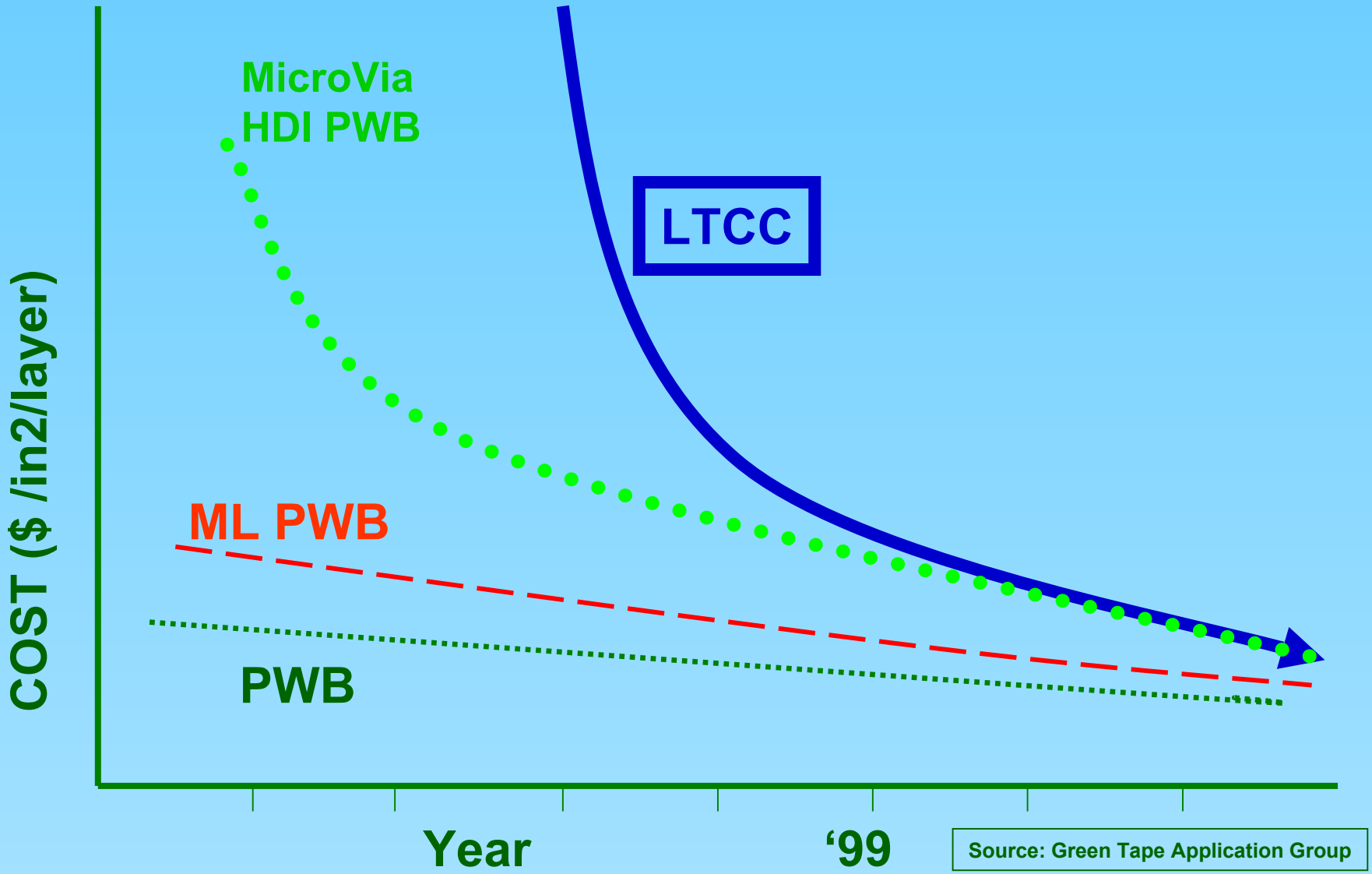
CERAMIC INTERCONNECT TECHNOLOGY



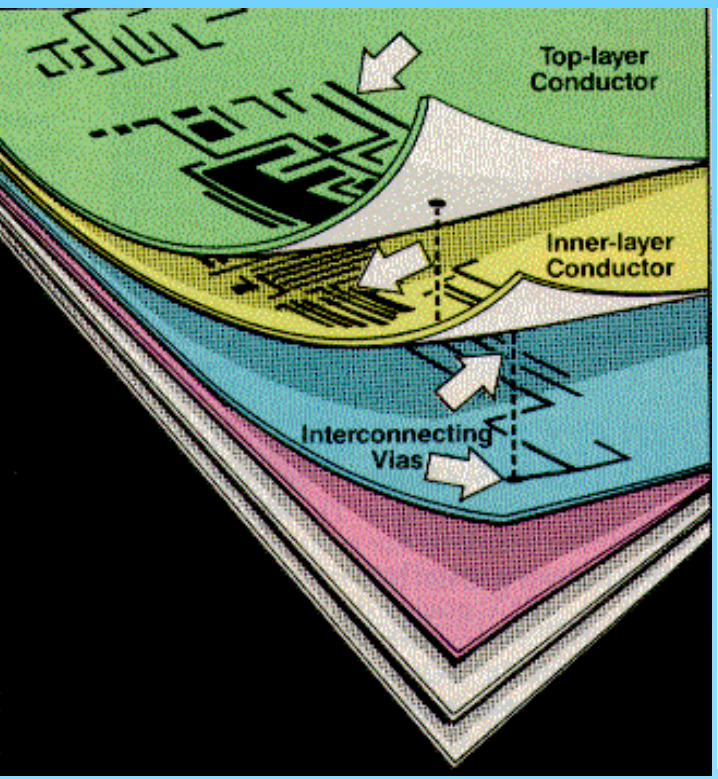
HYBRID CERAMIC TECHNOLOGIES

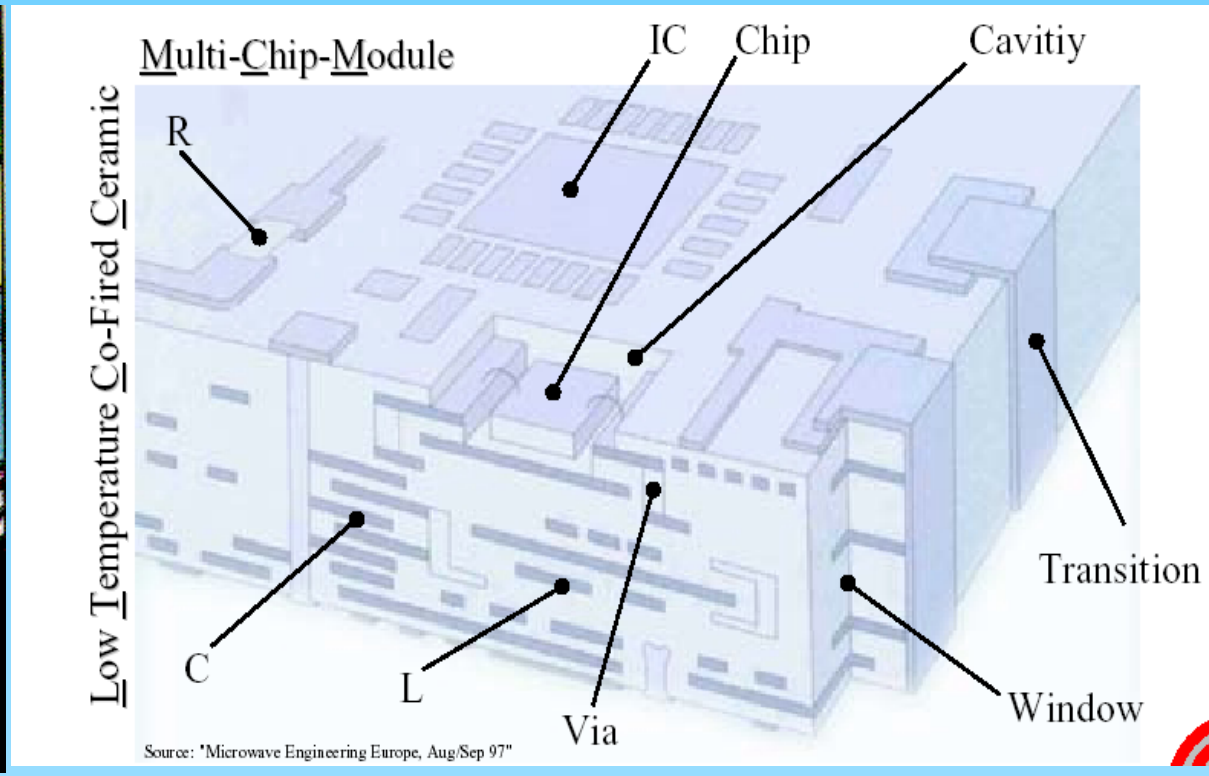


COST GAP NARROWS

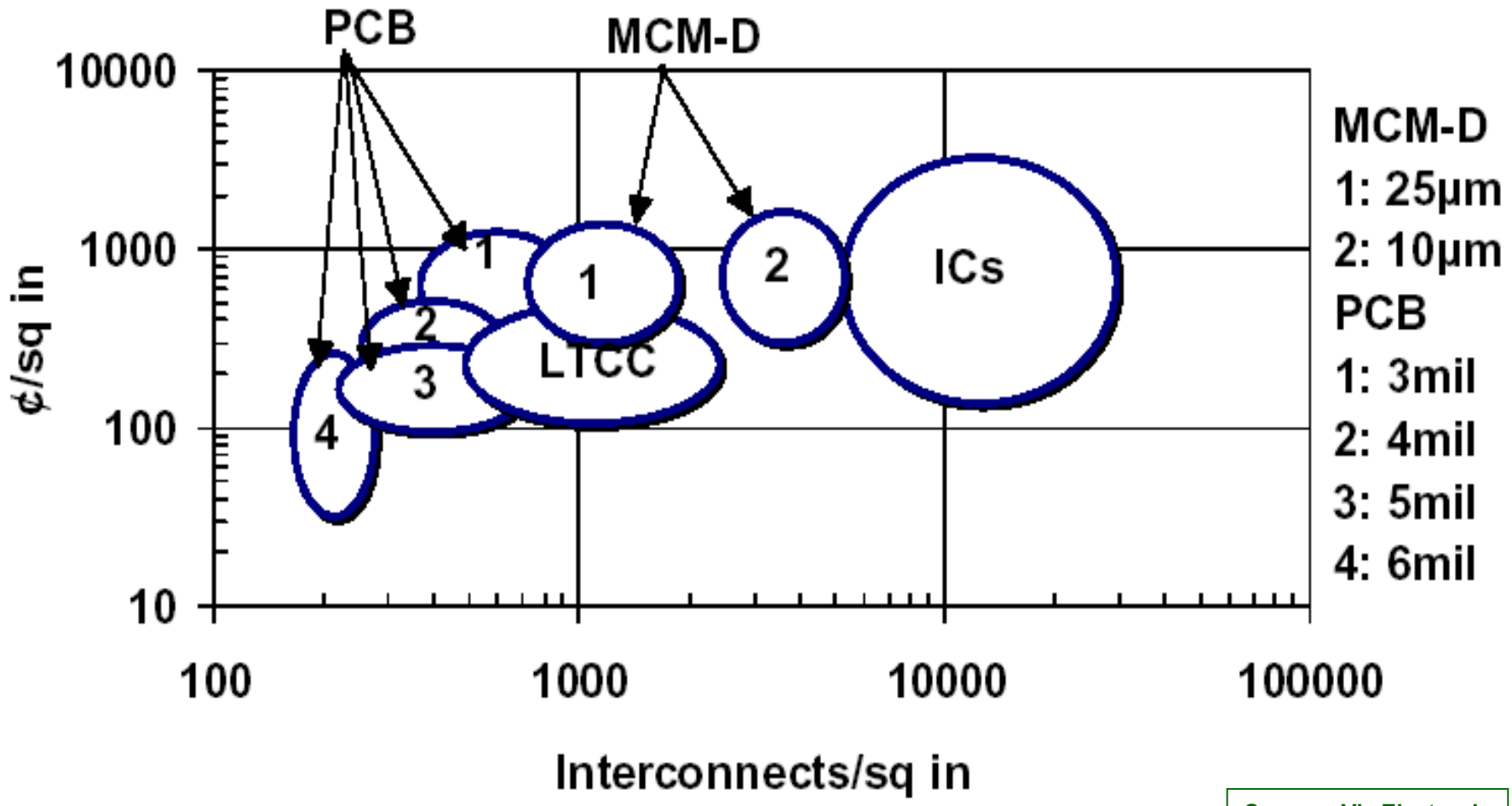


LTCC For MCM


Top-layer Conductor
Inner-layer Conductor
Interconnecting Vias


Multi-Chip-Module
Low Temperature Co-Fired Ceramic
IC
Chip
Cavitiy
R
Transition
C
L
Via
Window
Source: "Microwave Engineering Europe, Aug/Sep 97"

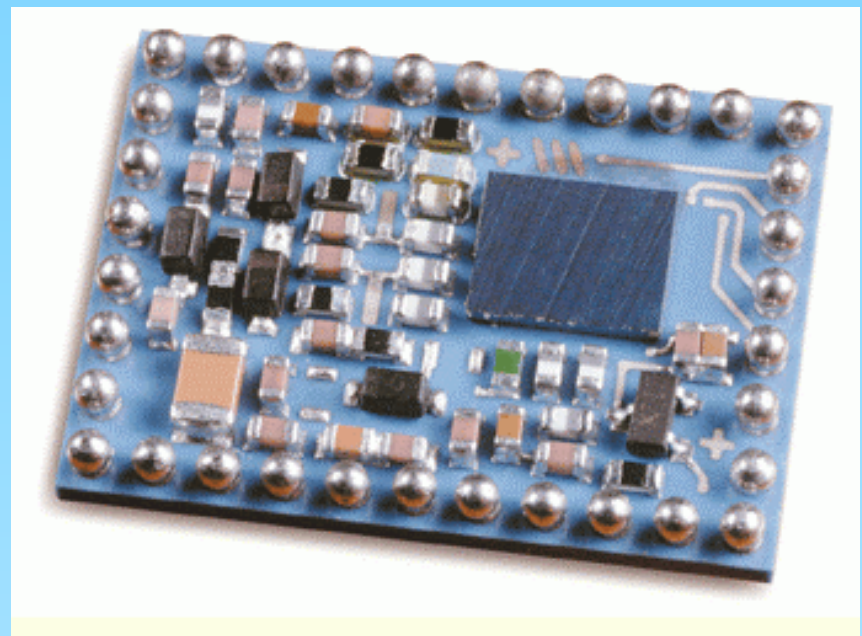
COST COMPARATION FOR MCM APPLICATIONS



Source: Via Electronic

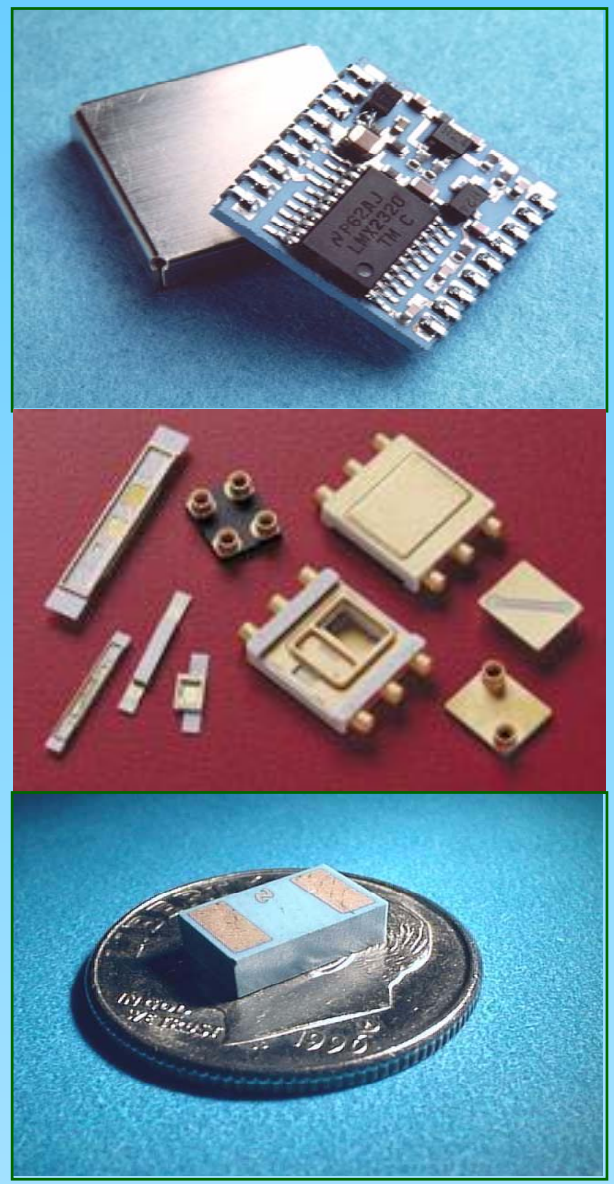
WHAT IS LTCC ?

- LTCC was originally developed by Hughes and DuPont for Military Systems.
- The (LTCC) technology can be defined as a way to produce multilayer circuits with the help of single tapes, which are to be used to apply conductive, dielectric and / or resistive pastes on.
- These single sheets have to be laminated together and fired in one step all. This saves time, money and reduces circuits dimensions. An other great advantage is that every single layer can be inspected (and in the case of inaccuracy or damage) replaced before firing; this prevents the need of manufacturing a whole new circuit.
- Because of the low firing temperature of about 850°C it is possible to use the low resistive materials silver and gold .
- The size of the LTCC board can be reduced considerably because of the 3D structure and passive components such as capacitors, inductors and resistors can be embedded, which facilitates a high degree of integration.



LTCC APPLICATIONS

- LTCC technology provides low-cost, high passive elements (R, L, C) integration and good electrical properties with the possibility to use silver, gold, palladium, platinum as conductors.
- This is not achievable with HTCC technology, where the firing temperature exceeds 1000°C, which is only compatible with tungsten or molybdenum conductors.
- The advantages of the LTCC technology make it suitable for a number of applications, i.e.:
  - RF Modules
  - Mobile phone
  - Blue tooth
  - Microwave & Opto-electronic modules
  - Automotive, Medical & Military
  - Sensor packaging
  - Microsystems



TECHNOLOGY ADVANTAGES (1)

– **Process**
  - Parallel process (high yield)
  - Single sinter step for all inner metallizations (cofiring)

– **Electrical**
  - Low k compared to HTCC
  - Low dielectric loss / no tremendous increase at microwave frequencies
  - Higher conductivity compared to HTCC (factor 2..4)
  - Number of signal layers almost unlimited
  - High wiring density (vias 2 - 4 x smaller than Thick Film vias)
  - Good control of dielectric layer thickness prerequisite for impedance control
  - Passive integration possible
  - Compatible to 7 decades of postfire resistors

– **Thermal**
  - High resistance against ambient working temperatures (up to 350°C)
  - Good thermal conductivity compared to PCBs (factor 10)
  - Good match to semiconductor TCE's

– **Mechanical**
  - Good ability to mechanical structuring (drilling, cutting, punching) in green state
  - High mechanical strength of interconnecting structures
  - Bare dice can be placed in cavities
  - Very good hermeticity of the substrate (substrate can be part of the housing)

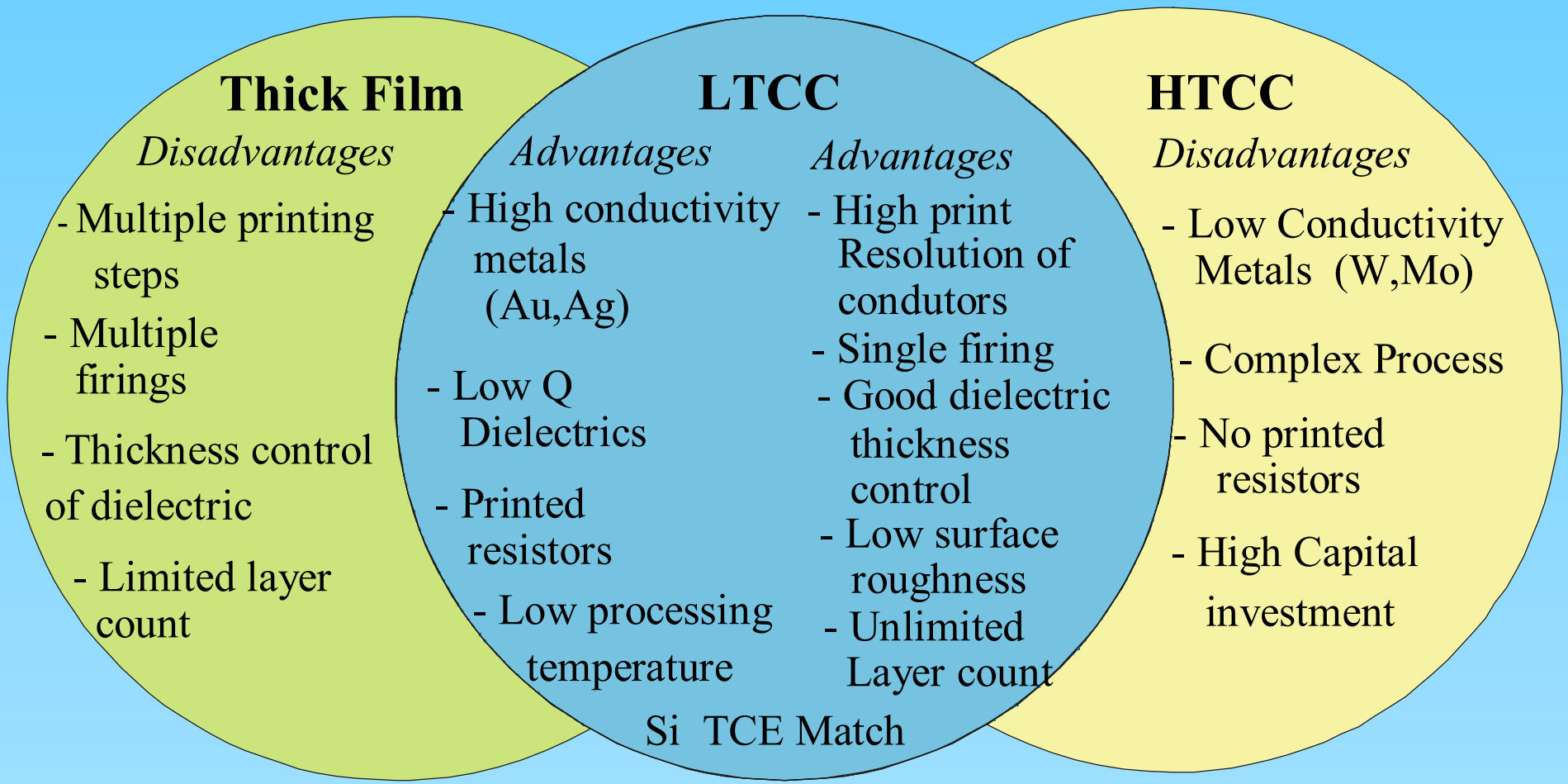
TECHNOLOGY ADVANTAGES (2)

- Low cost technology
  - Collective process adapted to automated manufacturing equipment
  - Only one firing step for all internal layers
  - Silver based conductors
  - Firing temperature below 1000°C
- High reliability
  - Ceramic based materials
  - Temperature range up to –55°C /+150°C
  - Hermetic dielectric
  - Low thermal coefficient of expansion
  - Compatibility with bare dies
- High flexibility
  - Compatibility with a wide range of assembly techniques
    - Bare dies: wire bonding, Flip chip,
    - Packaged devices: SMT
  - Packaging capability (PGA, LGA, BGA, QFP)
  - Complex shape of substrate
  - Cavities
- High electrical performance
  - Various tape thickness (35 to 210 µm): low parasitic line capacitance
  - Low resistivity conductor (Ag or Au – 3 mΩ/square)

TECHNOLOGY ADVANTAGES (3)

- High integration density
  - **Conductor linewidth and spacing down to 50 µm**
  - **Buried via structures (staggered and stacked)**
  - **Via diameter down to 150 µm (125 µm in local areas)**
  - **Via pitch down to 300 µm**
  - **High number of conductive layers: up to 24**
  - **Double sided substrate capability**
  - **Printed resistors (top or bottom)**
  - **Integrated packaging capability**
  - **Buried passive components**

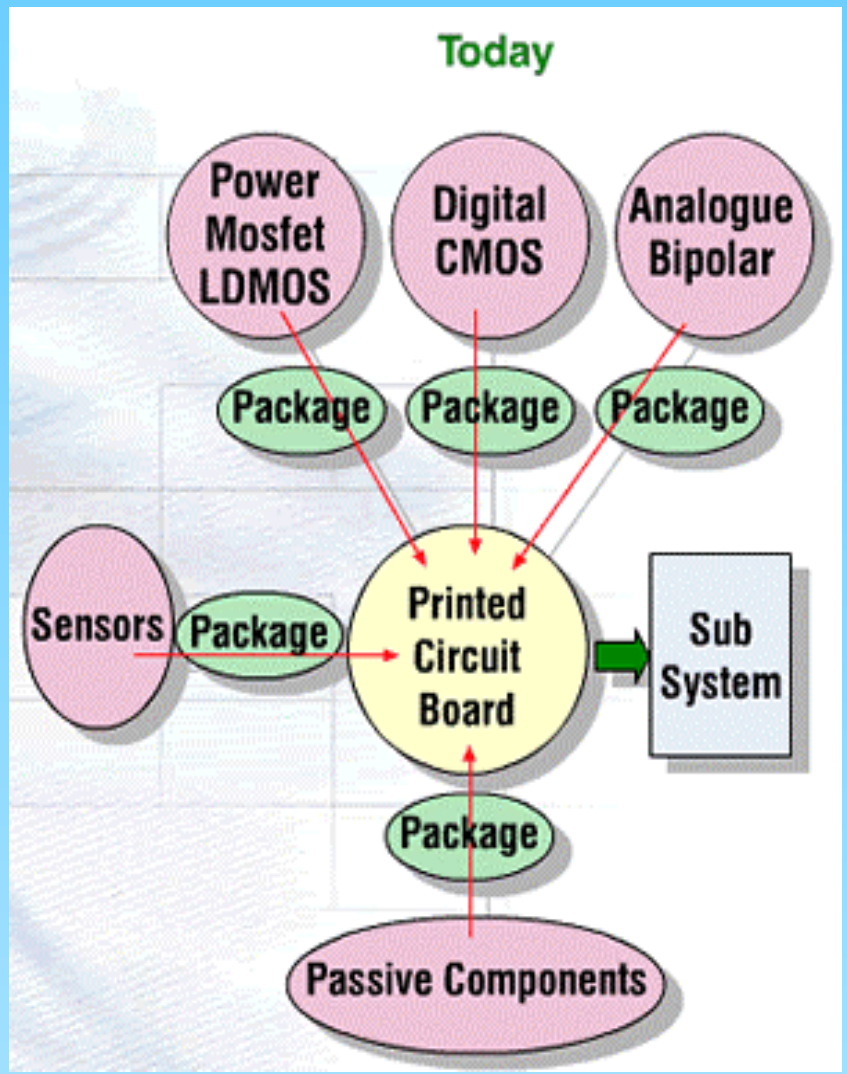
COMPARISON OF HYBRID CERAMIC TECHNOLOGIES

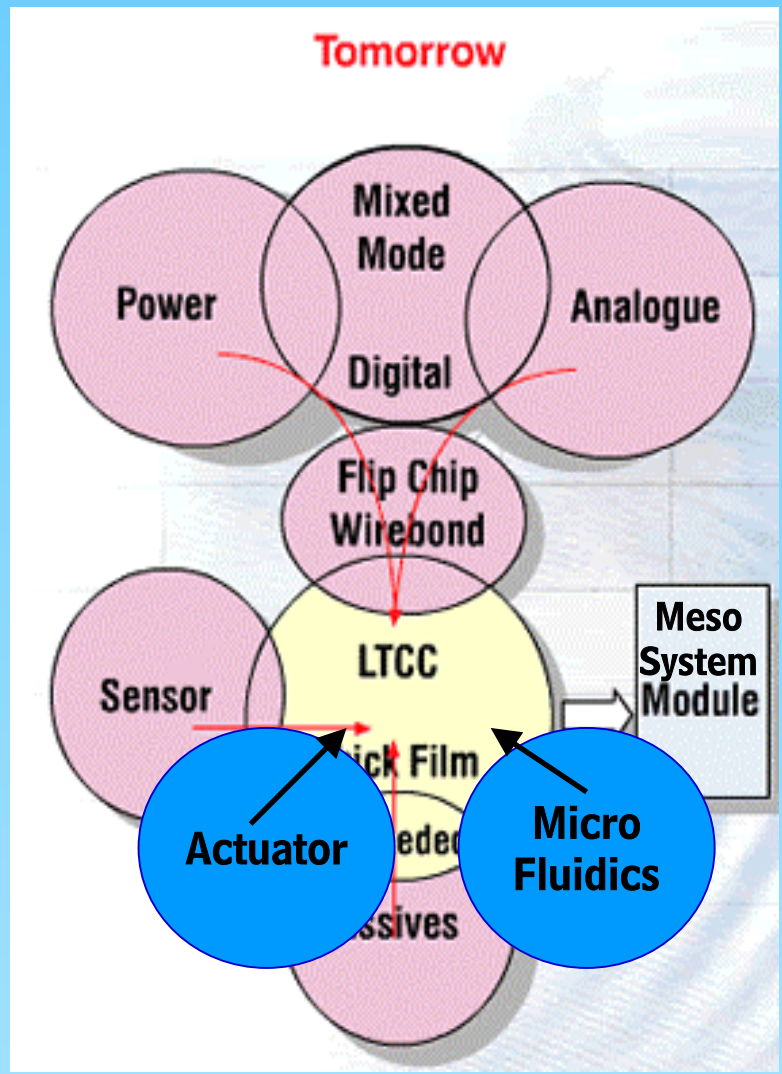


LTCC TAPE MATERIAL SUPPLIERS

- The following companies offer LTCC tapes for various applications.
  - **DuPont**
    - 951: k = 7.8 (standard tapes: CT, AT, A2, AX)
    - 943: k = 7.5 (low loss tape)
  - **ElectroScience Laboratories (ESL)**
    - 41110-25C: k = 4.0 – 5.0 (transfer tape: zero shrink)
    - 41010-25C: k = 7.2 – 8.2 (transfer tape: zero shrink)
    - 41020-25C: k = 8.0 – 10.0 (transfer tape: zero shrink)
    - 41110-70C: k = 4.3 – 4.7
    - 41020-70C: k = 7 – 8
  - **Northrop Grumman**
    - "Low K": k = 3.9
  - **Ferro**
    - A6M: k = 5.9 (microwave tape)
    - A6S: k = 5.9 (microwave tape)
  - **Heraeus**
    - CT2000: k = 9.1
    - CT700: k = 7.5 - 7.9
    - CT800: k = 7.5 - 7.9 (zero shrink tape)
  - **Kyocera**
    - GL550: k = 5.6 - 5.7
    - GL660: k = 9.4 - 9.5
  - **Nikko**
    - Ag2: k = 7.8
    - Ag3: k = 7.1
  - **Samsung**
    - TCL-6A: k = 6.3
    - TCL-7A: k = 6.8

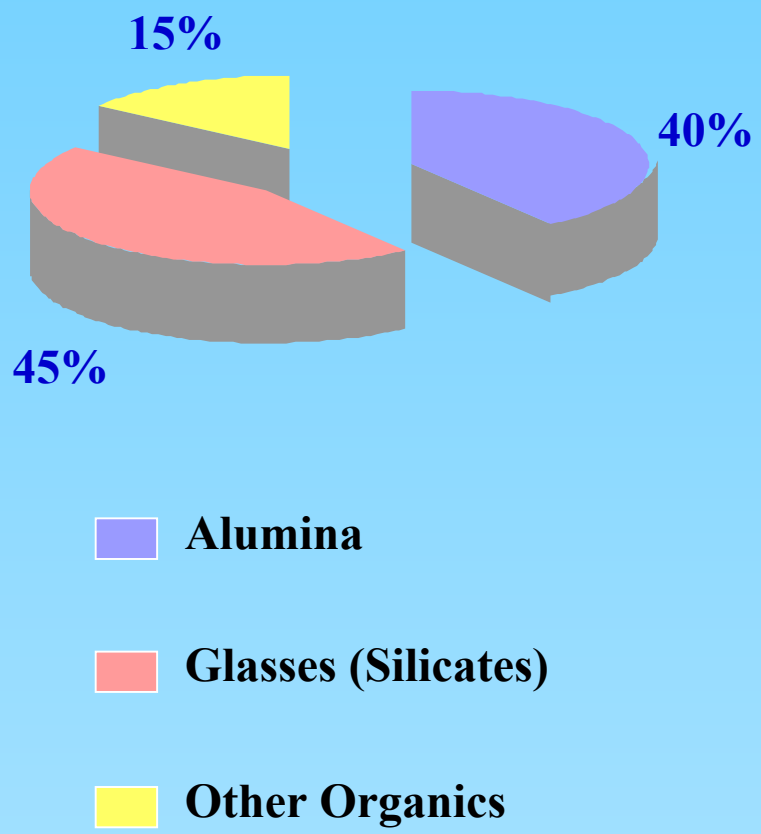
TECHNOLOGY VISION





LOW TEMPERATURE CO-FIRED CERAMICS (LTCC)

LTCC-951 Composition



- Glass-ceramic composite materials
- The ceramic filler is usually alumina, Al_2O_3
- The usual composition also includes a glass frit and an organic binder (plasticizer and anti-flocculant)
- Called green tape before firing and sintering

951 LTCC (DUPONT) DIELECTRIC TAPE

Typical Fired Properties

Electrical

Dielectric Constant (@ 10 MHz)	7.8
Dissipation Factor (@ 10 MHz)	0.15%
Insulation Resistance (@ 100 V DC)	>10^{12} OHM
Breakdown Voltage (V/25 µm)	>1000 V

Physical

Thermal Expansion (25°C-300°C)	5.8ppm/°C
Density	3.1 g/cm^3
Camber	Conforms to setter
Refire at 850°C	Stable
Surface Smoothness	0.22 µm
Thermal Conductivity	3.0 W/m-k
Flexural Strength	320 MPa

System Capability

Via Diameter Resolution	100 µm
Line/space Resolution	100 µm/100 µm
Maximum Layer Count	>80 layers

Unfired Properties

Thickness

951-AT	114 µm ±7% (4.5mils)
951-A2	165 µm ±7% (6.5mils)
951-AX	254 µm ±7% (10mils)

Shrinkage

(x,y)	12.27% ± 0.3%
(z)	15% ±0.5%

Tensile Strength	1.7 MPa
Young's Modulus	152 GPAS

LTCC 951 PASTES (DUPONT)

- Au 951 System
  - Cofired Inner Layer Conductor
    - 5734
  - Cofired Low Posting Via Fill
    - 5738
  - Cofired Top Layer Conductor
    - 5734 (Au Wirebondable)
    - 5739 (Pt/Au Solderable)
    - 5742 (Ag/Au, Al or Au Wirebond)
  - Braze Materials
    - 5062 Braze Adhesion Layer
    - 5063 Braze Barrier Layer
    - 5087 Au/Sn/Cu/Ag (Promote)
  - Buried Components
    - Capacitors
    - Resistors
  - Top Layer Post Fired Resistors
  - Post Fired Conductors

- Ag 951 System
  - Cofired Inner Layer Conductor
    - 6142 (Signal)
    - 6148 (Ground and Power)
    - 6145 (High Solids Ag)
  - Cofired Low Posting Via Fill
    - 6141
  - Cofired Top Layer Conductor
    - 6146 (Pd/Ag Solderable)
  - Braze Materials
    - 5081 Braze Adhesion Layer
    - 5082 Braze Barrier Layer
    - 5087 Au/Sn/Cu/Ag
  - Buried Components
    - Capacitors
    - Resistors
  - Top Layer Post Fired Resistors
  - Post Fired Conductors

PHOTO MATERIALS (DUPONT) FODEL

Multilayer Dielectric	6050
Gold Conductors	
Photoprintable	
Inner Layer	5956, 5956L
Top Layer	
(Au & Al wire bondable)	5956, 5956L
Silver Conductor (Top layer)	**6778**
Screen Printable	
Inner Layer	5715
Top Layer (1 mil Au wire bondable)	5715
Top Layer (2 mil Au & Al wire bondable)	5725
Via Fill	5727

LTCC MATERIAL PROPERTIES

COFIRED CERAMIC MATERIAL PROPERTIES		Ceramic Material System Du Pont 951		Ceramic Material System Ferro A6M
Ceramic Electrical Properties	Dielectric Constant at 1-2 GHz		7.8	5.9
	Dielectric Const. variation (± %)		± 2.5 ±1.5 (1)	± 2.5 ±1.5 (1)
	Fired layer thickness (µm) without/with stacked conductor local conditions	AX P2 PT C2	203/193 132/122 91/85 42/38	185 93
	Layer Thickness variation (± %)	951 AX & P2 951 PT & C2	± 5 ± 3	± 4 ± 2 (1)
Ceramic Thermal properties	Thermal Expansion Coeff. (ppm/C)		5.8	7
	Thermal Conductivity (W/mK)		3 (2)	2 (2)
Ceramic Physical Properties	Flexural Strength (MPa)		320	170
	Young Modulus (GPa)		150	92
	Surface Roughness RMS (µm)		0.7	0.7
	Unfired Panel Sizes at production (X x Y dimensions)		6" x 6"	6" x 6"
	X-Y Shrinkage % (± variance %)		12.7 ± 0.2	15
	Z Shrinkage % (± variance %)		15 ± 0.5	26
	Colour		Blue	White

LTCC MATERIAL PROPERTIES

Conductor properties	Ceramic Material System Du Pont 951	Ceramic Material System Ferro A6M
Conductor type(s)	Inner Ag External Ag, Au, PdAg [1]	Inner Ag External Ag, Au, PdAg [1]
Conductor thickness(µm) On Top layer	10 ±3	10 ±3
Conductor thickness(µm) On Buried Layer	10 ±3	10 ±3
Resistivity mΩ/□ Top layer (10 µm thick)	Au <4 Ag <3 AgPd <30	Au <4 Ag <3 AgPd <30
Resistivity mΩ/□ Buried layer	Ag <3	Ag <3
Conductor Roughness (Rq µm RMS) on Top layer (after fire)	Au : 0.8 Ag : 0.9	Unavailable
Conductor Roughness (Rq µm RMS) in buried layer (after fire)	Ag : 1.3	Unavailable
Minimum/Recommended Minimum line/space in µm/µm	75/100 minimum 75/100 recom.	75/100 minimum 75/100 recom.
Top Cofired Conductor linewidth tolerance (µm)	± 15	± 15
Inner Cofired Conductor Linewidth tolerance (µm)	± 15	± 15
Adhesive strength of top conductor N/mm^2	10 min [2]	3.5 min [2]

LTCC MATERIAL PROPERTIES

COFIRED CERAMIC RESISTIVE MATERIAL PROPERTIES

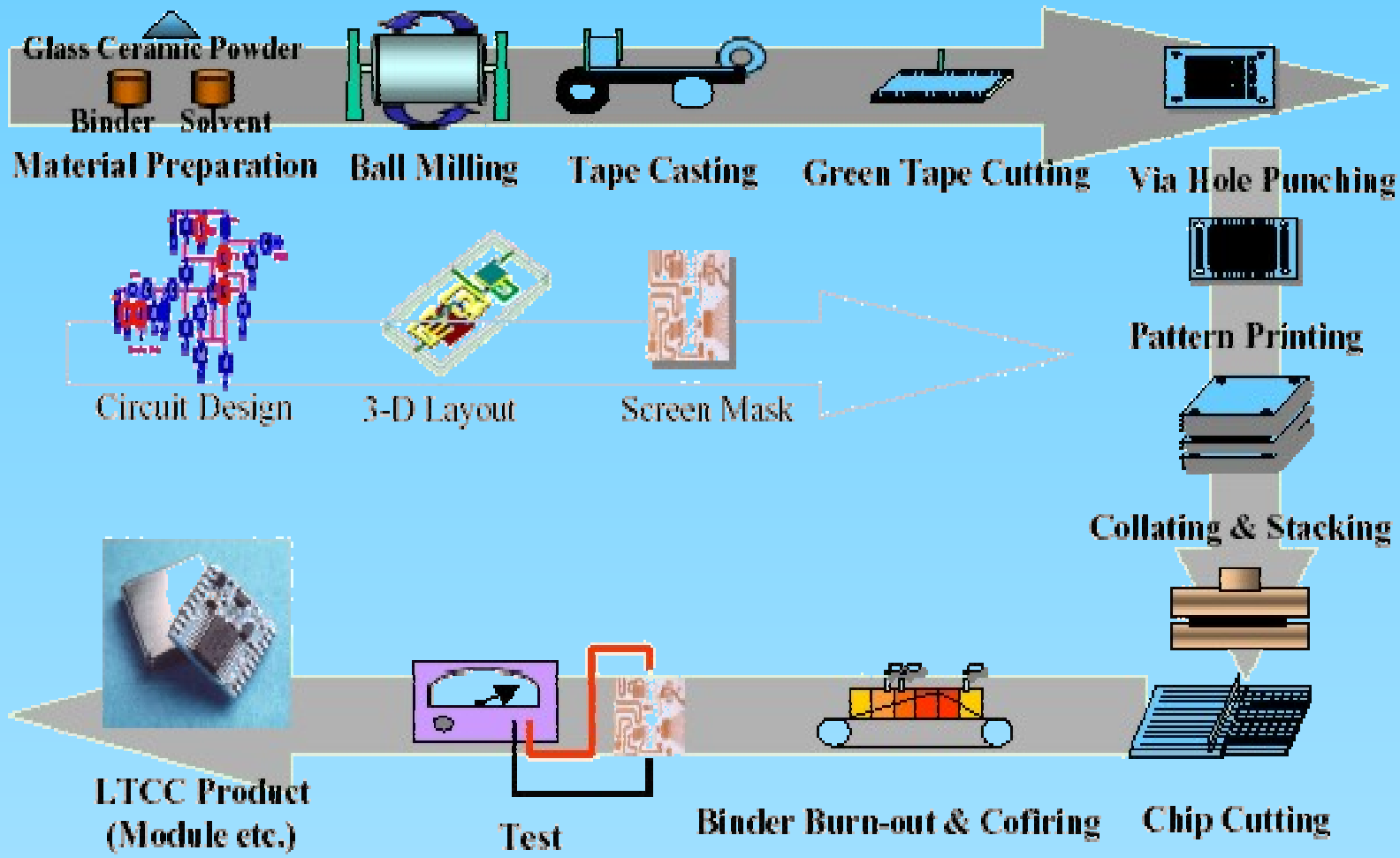
Resistor paste properties	Ceramic Material System Du Pont 951	Ceramic Material System Ferro A6M
Range of resistivity Ω/□	10 to 10^6 (External layers)	10 to 10^4 (Inner layers)
Thermal coefficient of resistivity (ppm/°C)	150 (≤ 100 KΩ/□) 200 (> 100 KΩ/□)	450 (≤00 Ω/□) 200 (>100 Ω/□)
Top layer postfired resistance tolerance %	± 30 ± 5 (1)	± 30 ± 5 (1)
Inner layer cofired resistance tolerance %	± 50	N/A

Capacitive paste properties	Ceramic Material System Du Pont 951 (1)	Ceramic Material System Ferro A6M (1)
Range of capacitance pF/mm^2	1.92	0.56
Inner layer cofired capacitance tolerance %	± 15	± 10

LTCC PROCESSING

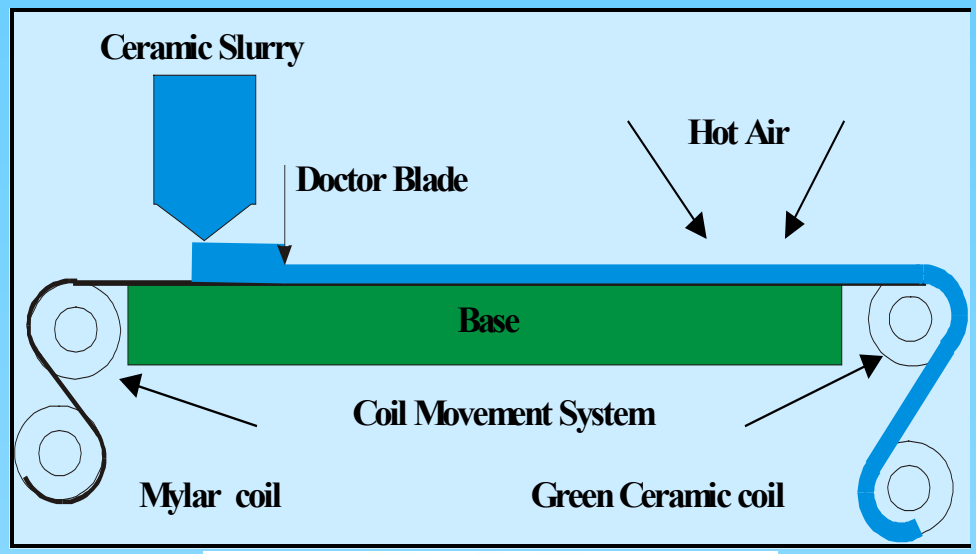
- **Processing steps**
- **Tape Machining**
  - **Punching, CNC, Laser & JVE**
- **Lamination**
- **Sintering**
- **Bonding to other materials**
- **Sagging Problem**

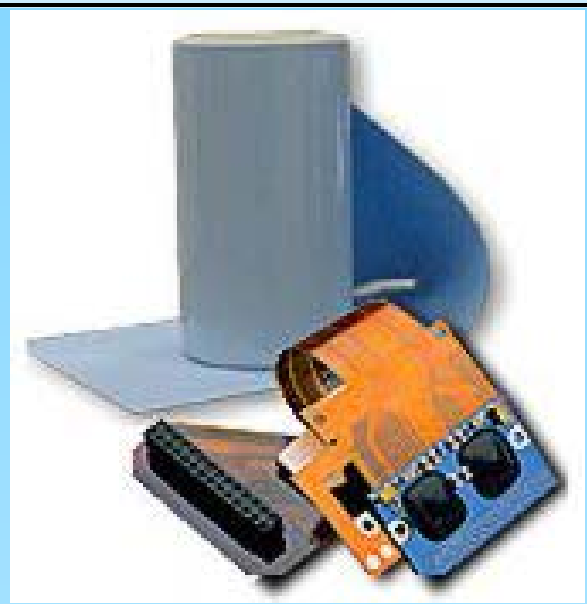
LTCC PROCESSING SCHEDULE



LTCC MANUFACTURING PROCESS (1)

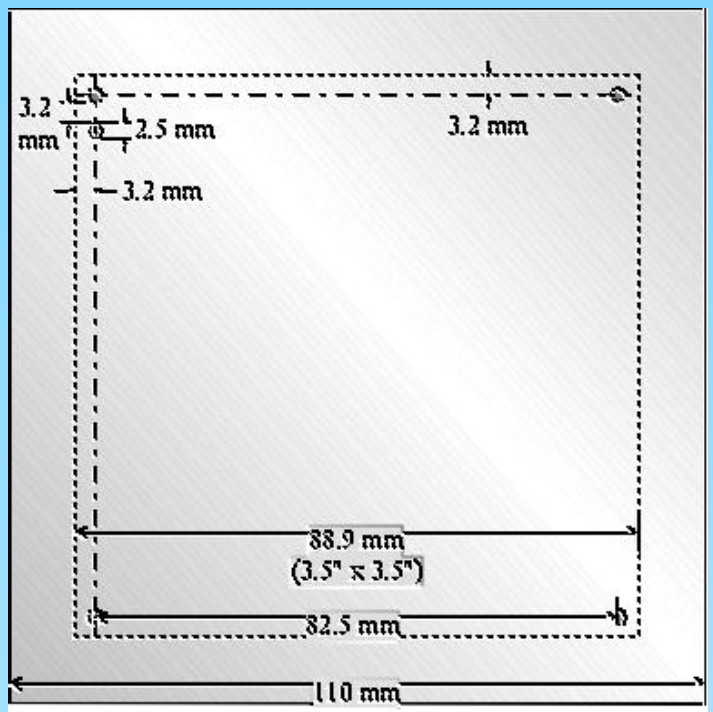
- Materials Preparation
  - LTCC Ceramic tape materials are prepared by milling precise amounts of raw materials into a homogeneous slurry.
  - This mixture is principally of ceramic/glass powders with controlled particle sizes with fluxes and small amounts of organic binders and solvents.
  - This slurry is poured onto a carrier and then passed under a blade to produce a uniform strip of specific thickness.
  - When dried, this strip becomes a ceramic-filled "Green ceramic tape" which is easily handled in rolls or sheets for unfired processing.



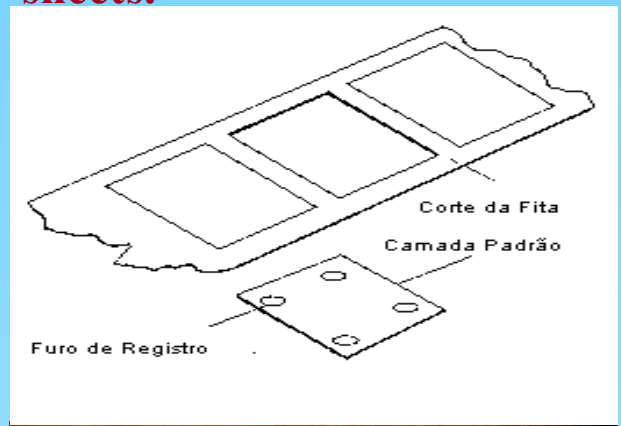


LTCC MANUFACTURING PROCESS (2)

- Tape Preparation
  - Cutting tape
  - Pre-Conditioning in the furnace
  - Punching or burning registration holes
  - Removing Mylar-tape

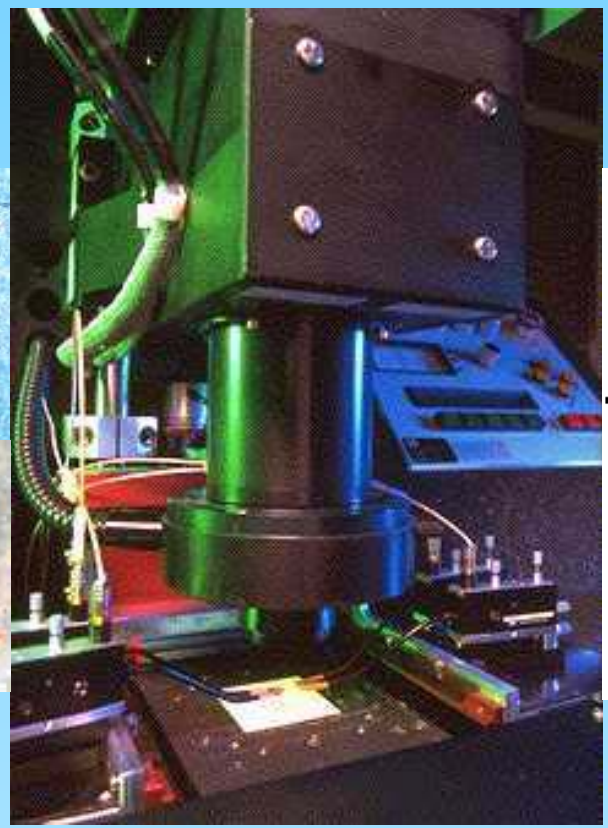


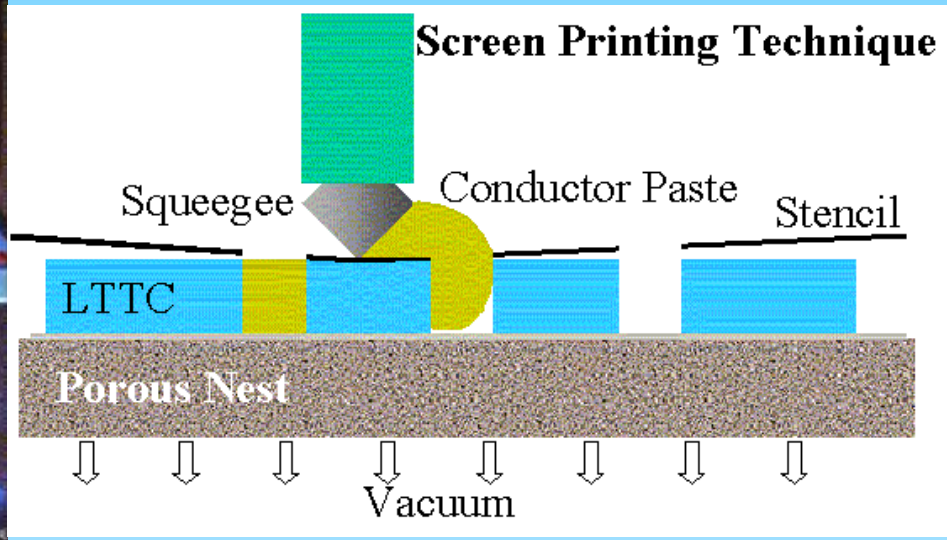
- Blanking
  - A blanking die is used to create orientation marks and the final working dimension of the green sheets.



LTCC MANUFACTURING PROCESS (3)

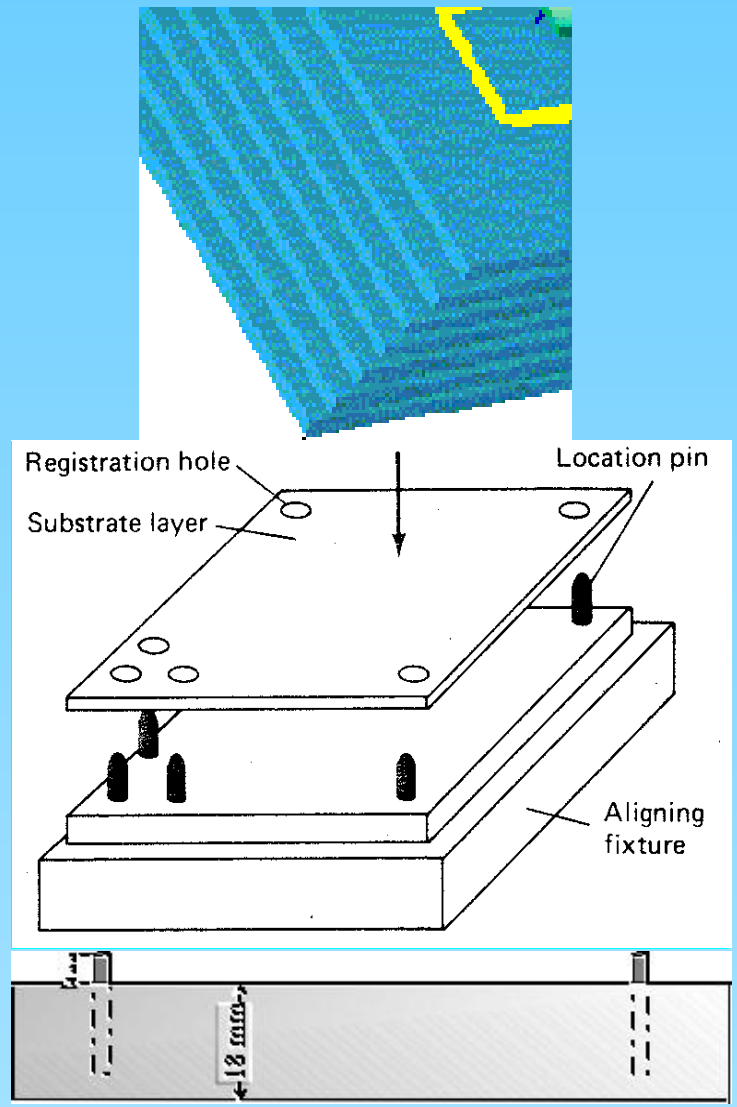
- Via Machining
  - Using high-speed mechanical punching with a matrix tool, Laser System, CNC or JVE.
- Via Filling
  - Performed using an thick film screen printer with a stencil metal mask.
  - Registration is performed using a vision system.





LTCC MANUFACTURING PROCESS (4)

- Paste Printing
  - Resistor, conductor and dielectrics deposits are performed using an automatic thick film screen printer with mesh screens.
- Collating
  - All layers will be collated and stacked with a special tool and will be fixed together to avoid misalignment.
  - Can be performed using a vision system for alignment.

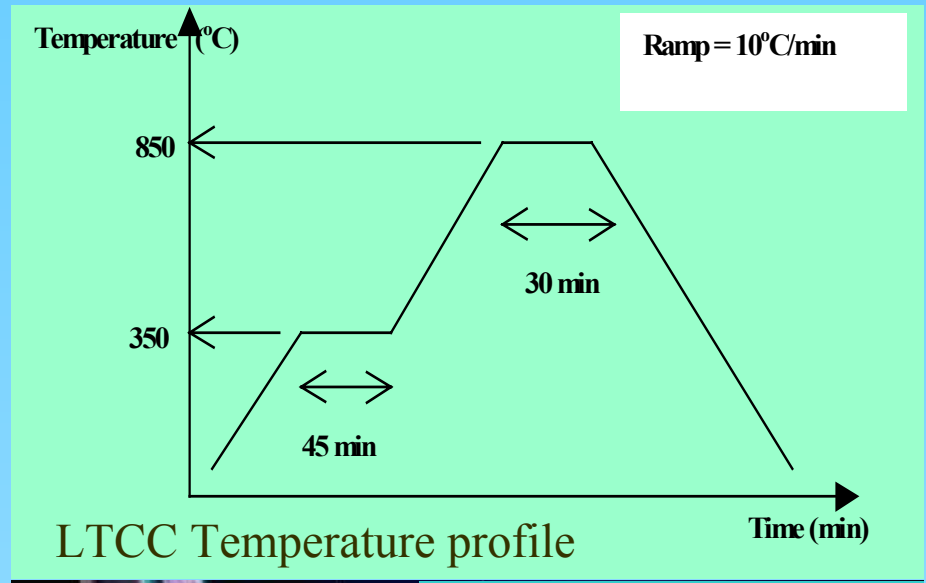


LTCC MANUFACTURING PROCESS (5)

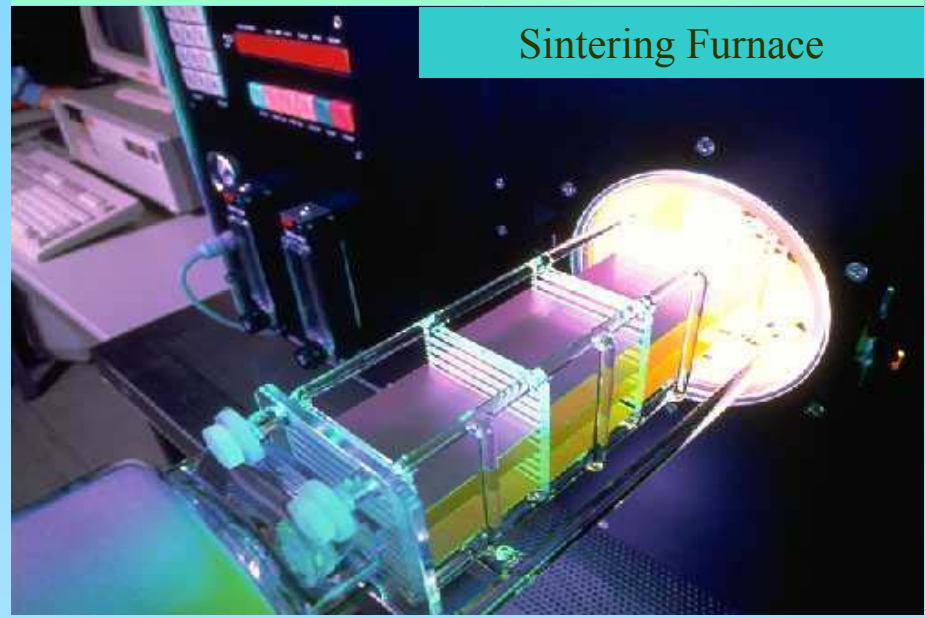
- Laminating
  - Accomplished using uniaxial or isostatic lamination in a specially designed press.
  - Typical cycle time is 10 minutes. The range of laminating pressure is from 200 to 300 bar.
- Pre-Cutting
  - Laminates are pre-cut with a hot blade, meeting the panel drawing specifications.

LTCC MANUFACTURING PROCESS (6)

- Co-Firing
  - Made in a belt or special furnace at a peak temperature of 850°C and a dwell time of 15 minutes.
  - The typical cycle time is 3 hours.

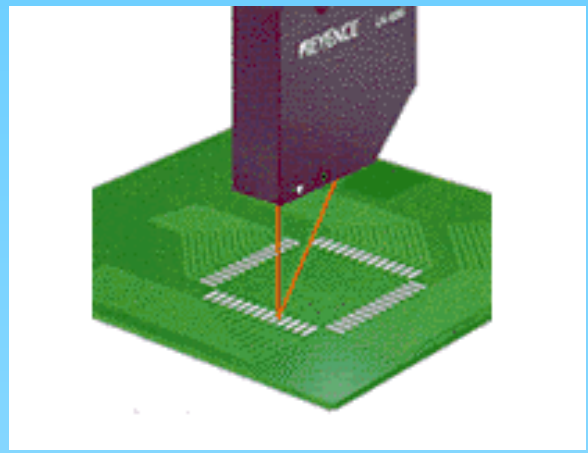


LTCC Temperature profile


Sintering Furnace

LTCC MANUFACTURING PROCESS (7)

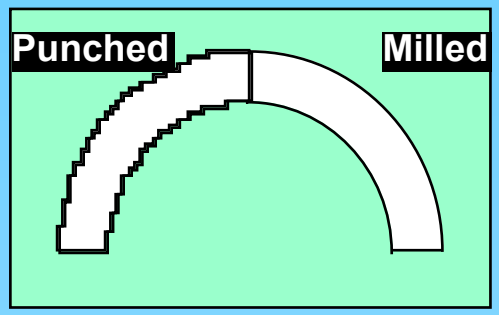
- Dimensional Measurements /Electrical Test:
  - Panel and circuit size can be checked with automatic measurement vision system. Electrical resistance test is performed with an automatic system with probe card.

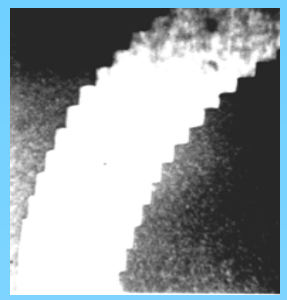


- Final Inspection:
  - Optical, Laser and acoustic inspection techniques are performed on completed parts in accordance with the applicable standards.

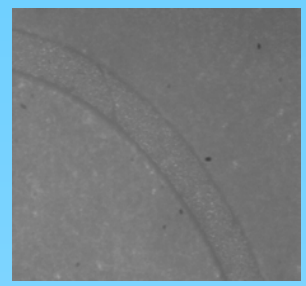
Mechanical Machining of Ceramic Tapes

Machined Samples

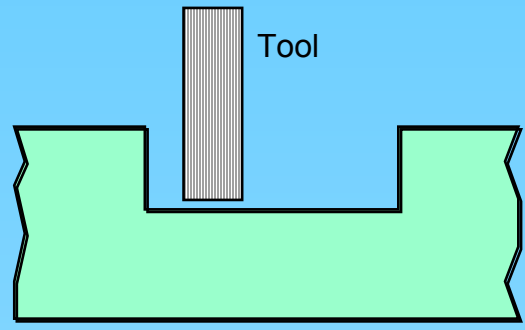




Punched curve



CNC milled curve
(two layered structure; the curved slot is in the top layer only)



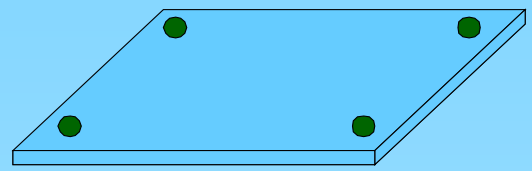
Partial depth CNC milling

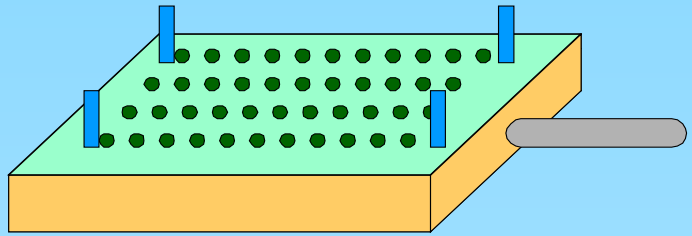
PUNCHING

- Circular or square shape
- Smallest size 0.004”(~100microns)
- Machining of curved features is difficult
- Partial depth machining cannot be done

CNC MILLING

- Smallest size 0.005”(~125microns)
- Machining of curved features is easy
- Partial depth penetration facilitating shallow channels and thin membranes
- Vacuum chuck holder or wet tape is used to fix tape

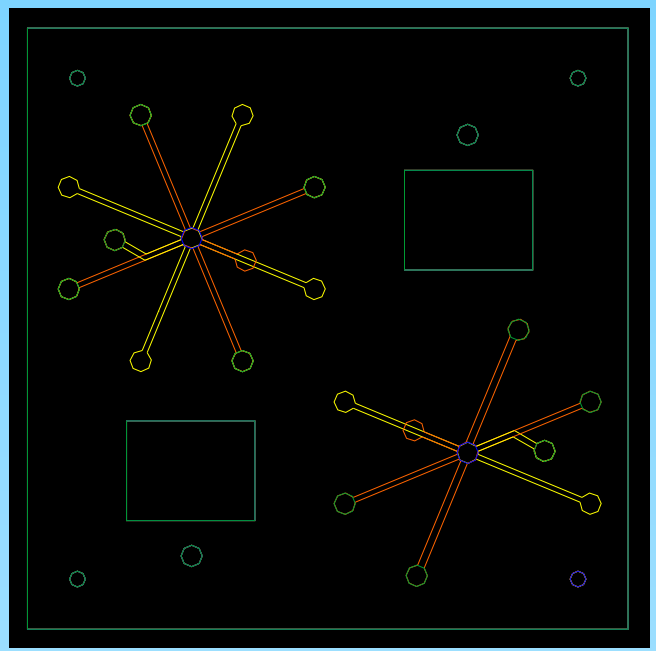


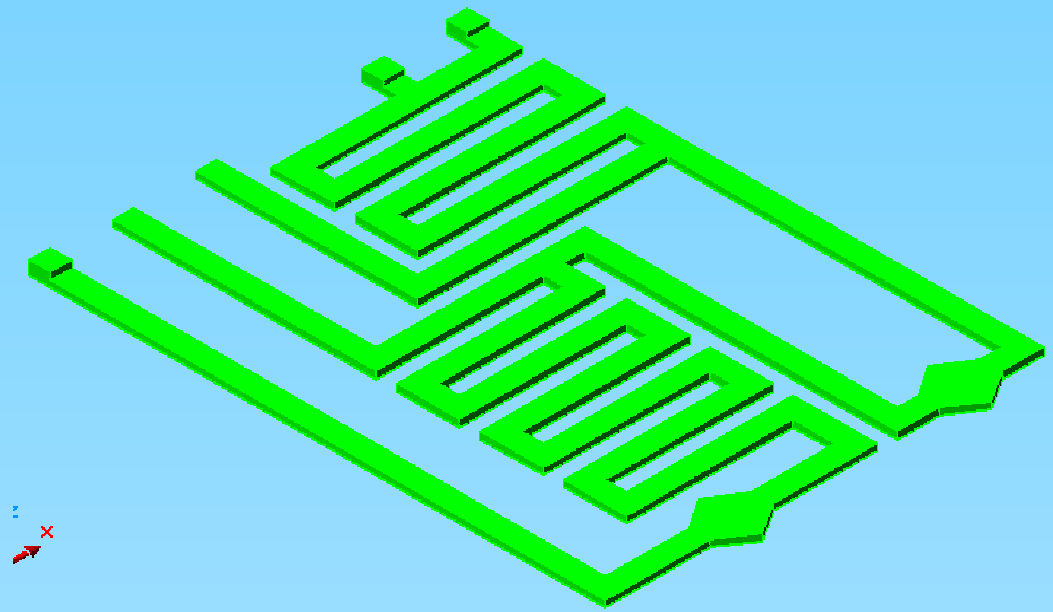


Vacuum chuck holder for CNC milling

GREEN TAPE MACHINING

Computer Assisted Design of the desired structures



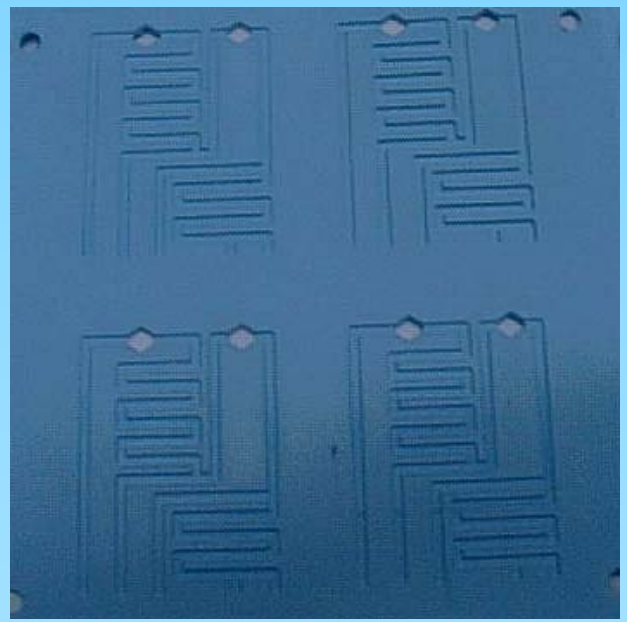


CNC PROCESS

- The machining of LTCC tapes was performed using a CNC (Computer Numerical Control) equipment (ProtoMat®C100/HF).

This equipment has as its main application the prototyping of printed circuit boards, but it can be simply adapted to be used for LTCC machining in the meso scale.

Channel Structure Low Relief Structure



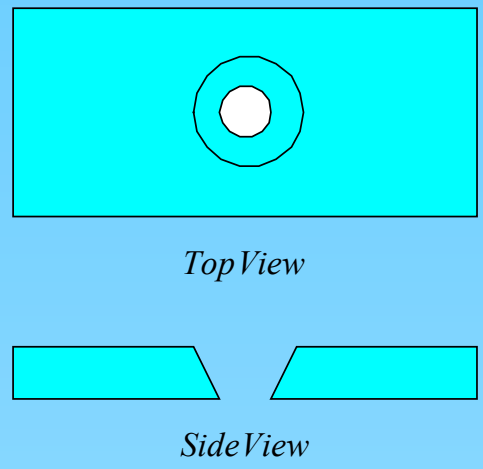
LASER MACHINING OF CERAMIC TAPES

Nd-Yag Laser

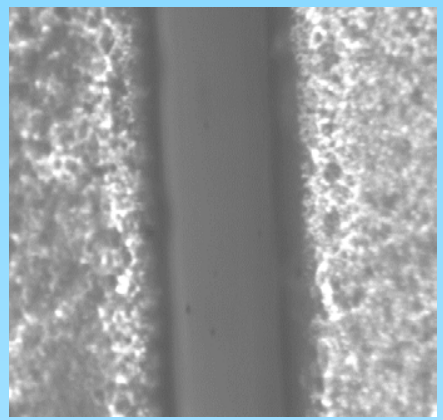
- Thermal machining process

Excimer Laser

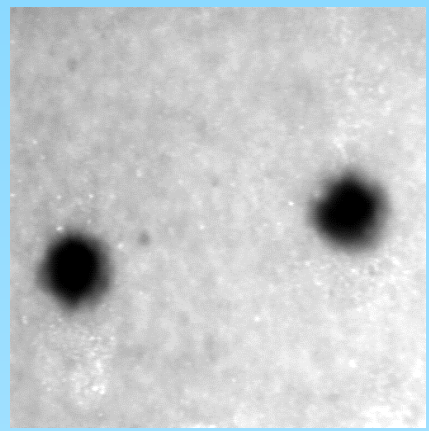
- Smallest size: ~10 microns
- No thermal damage (adiabatic process)
- Machining of whole feature at once using mask
- Partial depth penetration facilitating shallow channels and thin membranes



Schematic of the Laser machined hole



Nd-Yag Laser machined sample
(~150 micron wide channel, 20X)

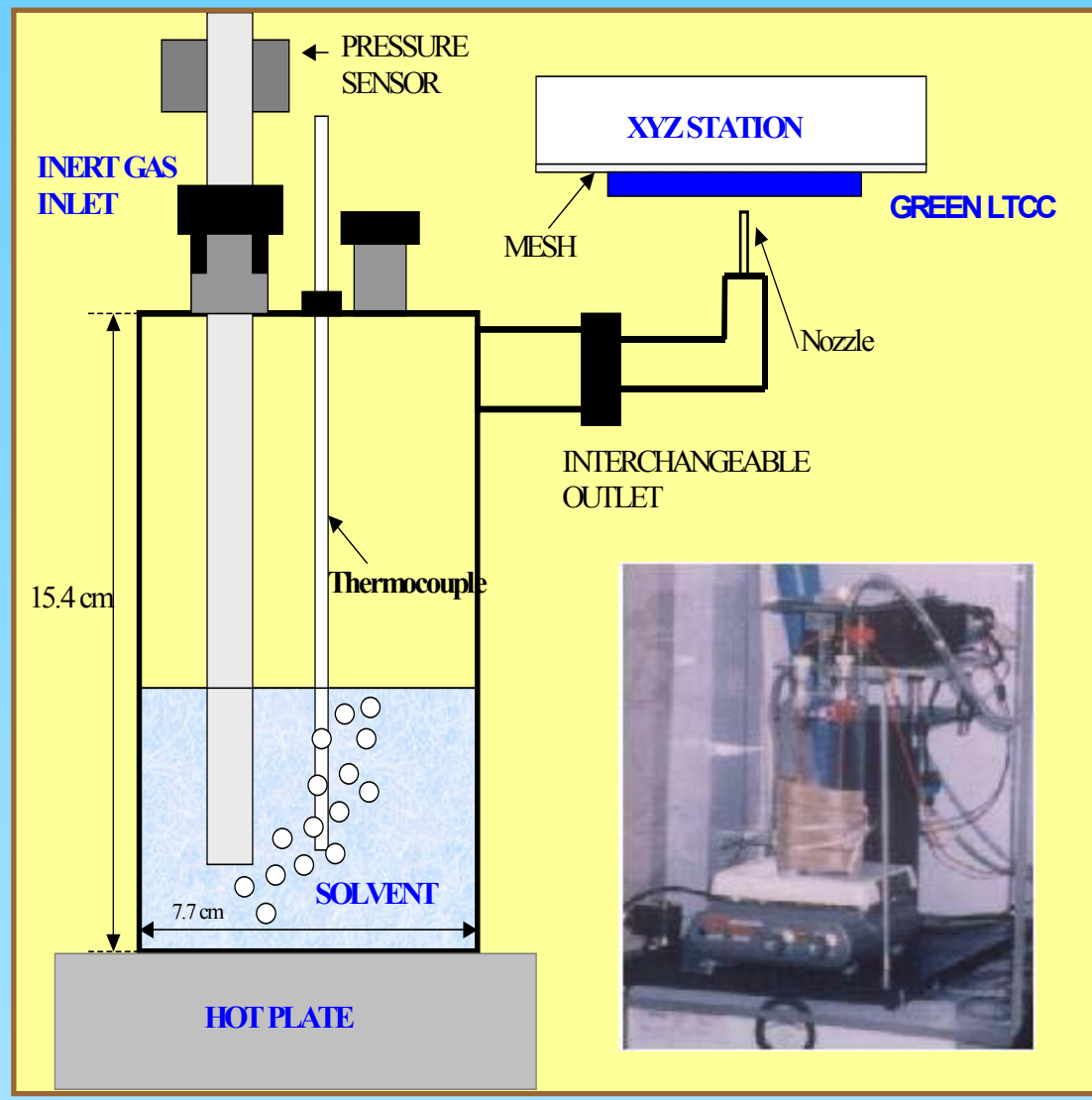


Excimer Laser machined sample
(~ 40 micron holes, 20X)

Yag Laser Machined Via

TAPE JET VAPOR ETCHING

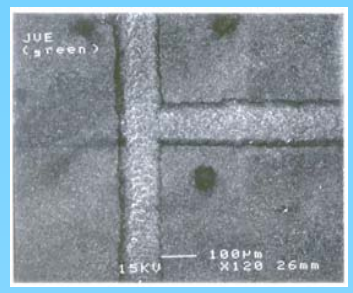
- A jet of acetone dissolves the organic binder
- The alumina grains are removed by momentum transfer
- Computer controlled xyz station and valves
- Morphology controlled by processing parameters: pressure, temperature, distance to sample, solvent, nozzle size and diameter

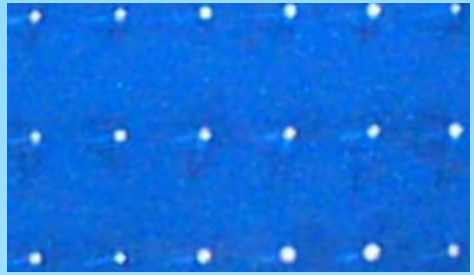


ADVANTAGES OF JET VAPOR ETCHING

- Rapid prototypes
  - **More flexible than traditional punching technique**
    - **One can do partial cavities and continuous borders when machining long channels**
  - **Processing and instrumentation costs are a fraction of conventional punch and die process**

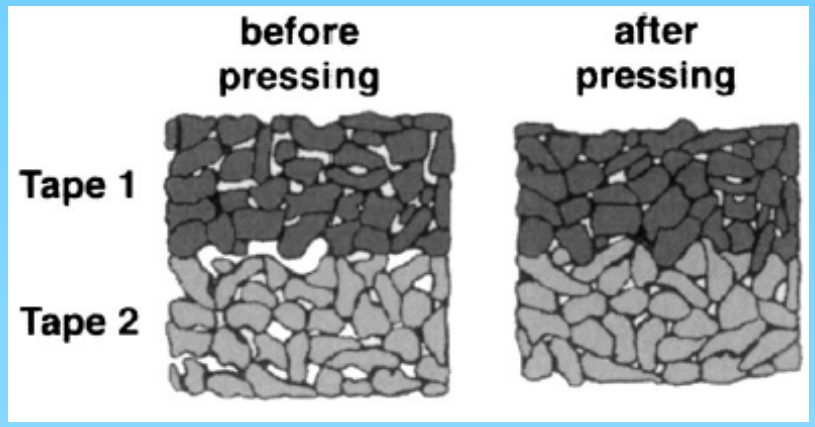
Features as small as 10μm has been obtained



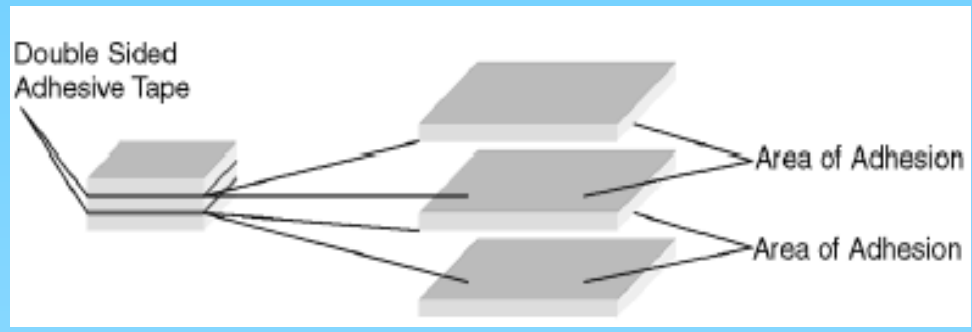


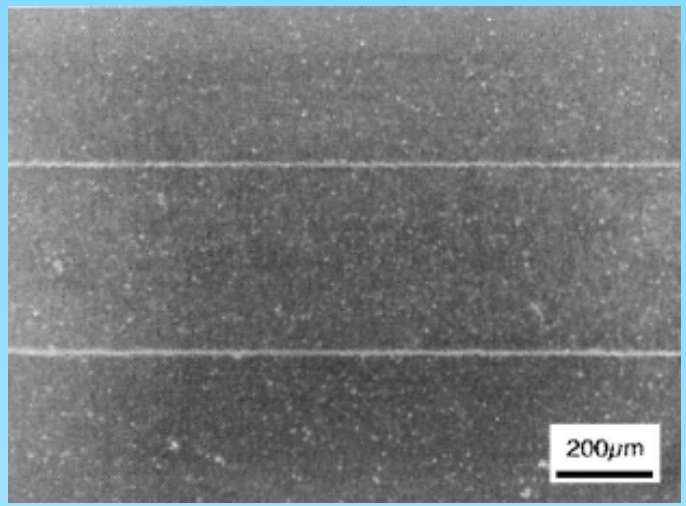
LAMINATION PROCESS

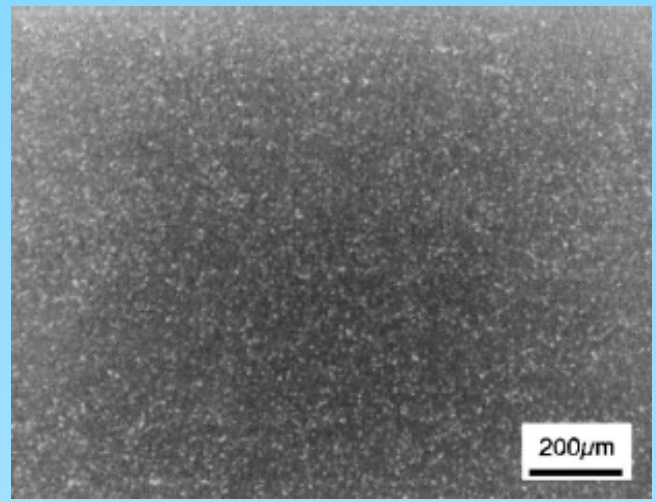
Thermocompression



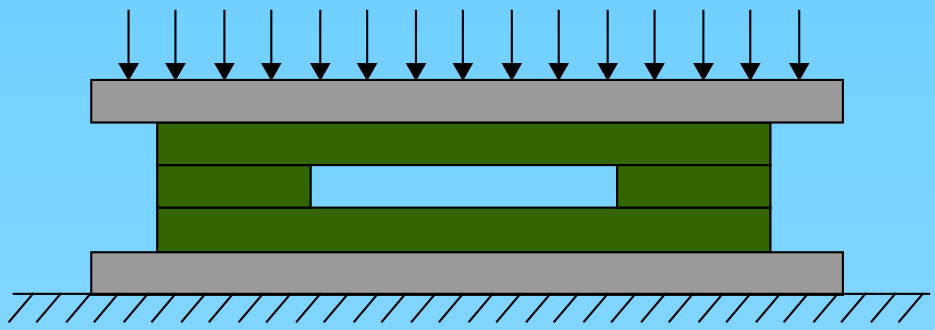
Cold Low Pressure





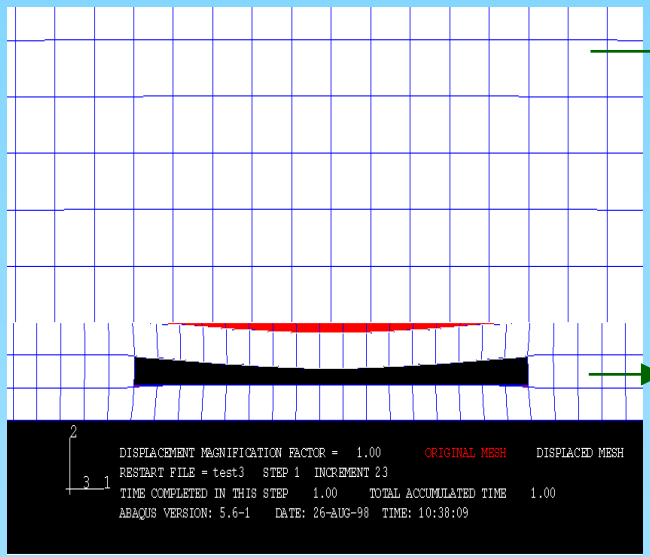


LAMINATION INDUCED DEFORMATION

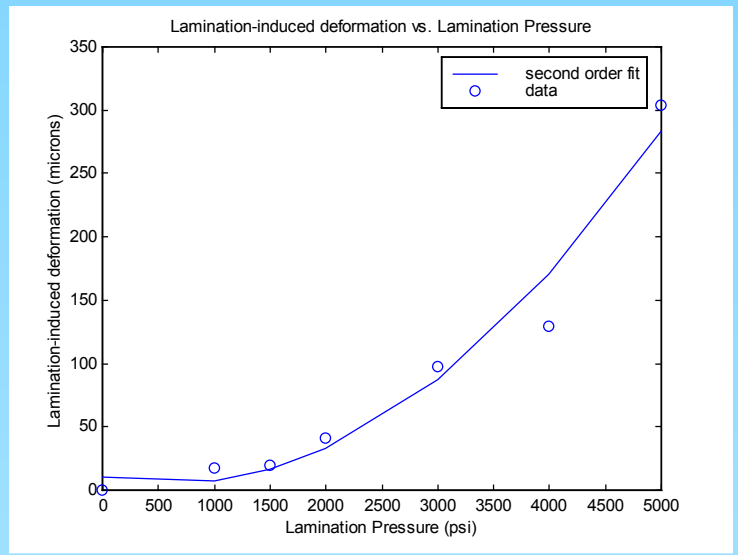


Lamination pressure = 3000 psi

Sample deformed under pressure



ABAQUS FEA Simulation

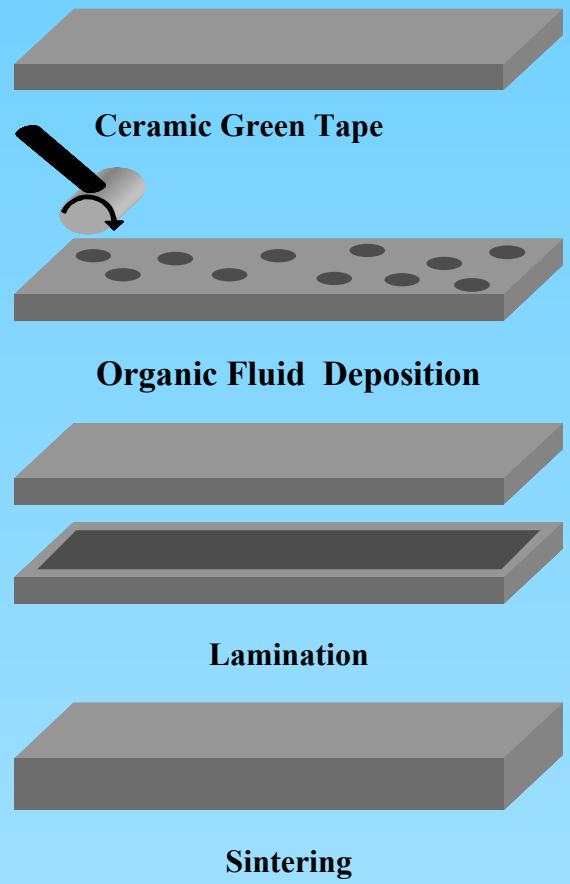


Maximum deformation (μm)

Lamination pressure (psi)

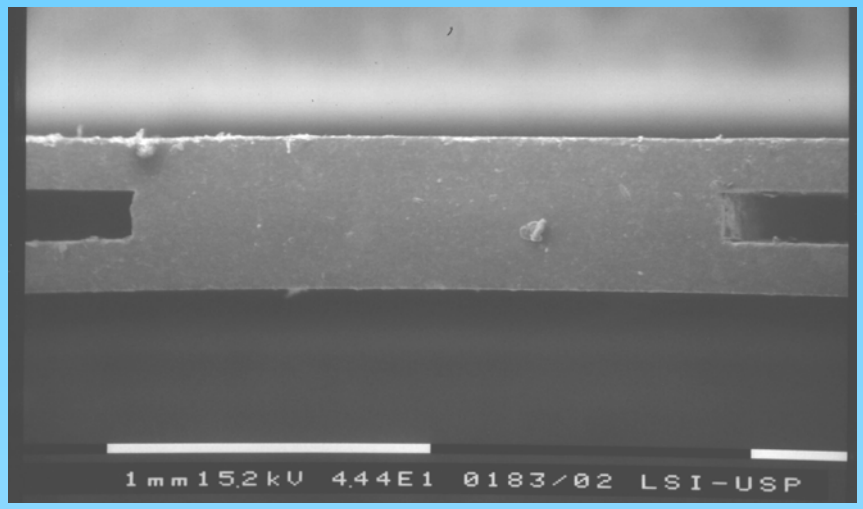
LOW TEMPERATURE AND PRESSURE LTCC LAMINATION USING ORGANIC FLUIDS

- Advantages of lamination using organic fluids :
  - **–Excellent gluing function and easy tapes alignment in room temperature due to their high viscosity;**
  - **–Low pressure and temperature process;**
  - **–No pressure gradients in laminate;**
  - **–Easy method of deposition, allowing lamination of complex shapes and non-uniform surfaces;**
  - **–Sintering temperature profile with high heating rate compared with CLPL method;**
  - **–Organic fluid deposition can be realized by dipping, screen printing or dispensing techniques**

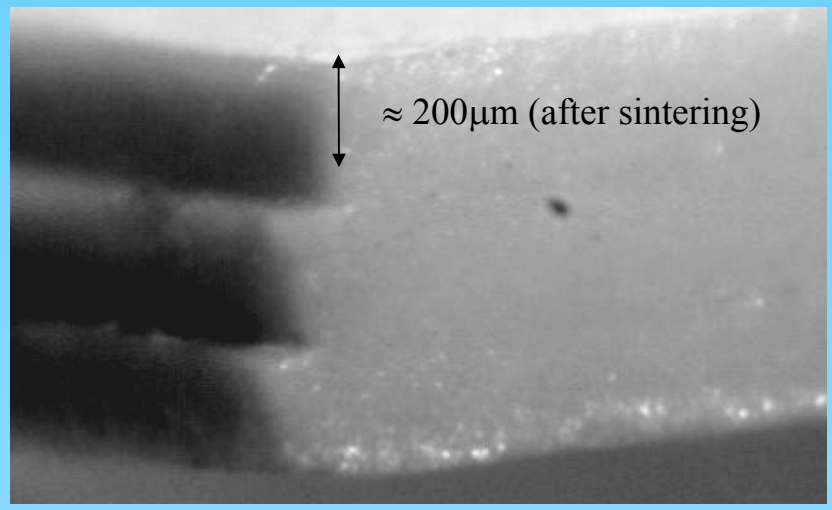


LAMINATION RESULTS

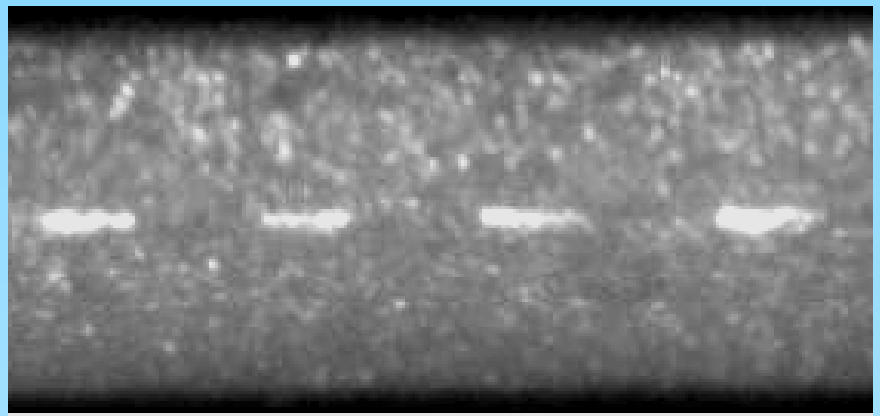
SEM of Channels



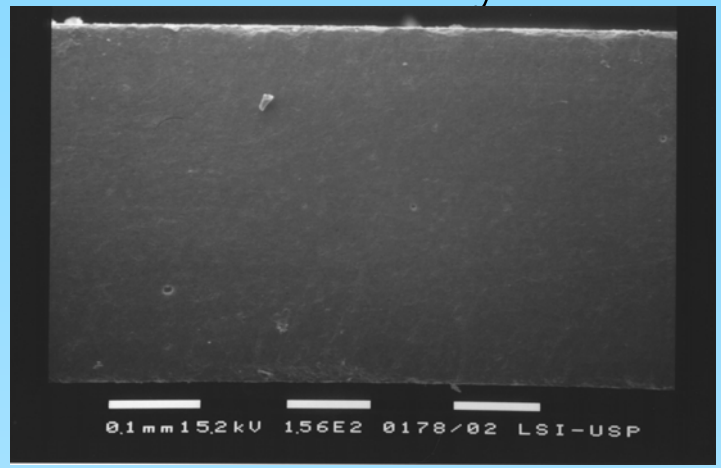
Three layer Lamination



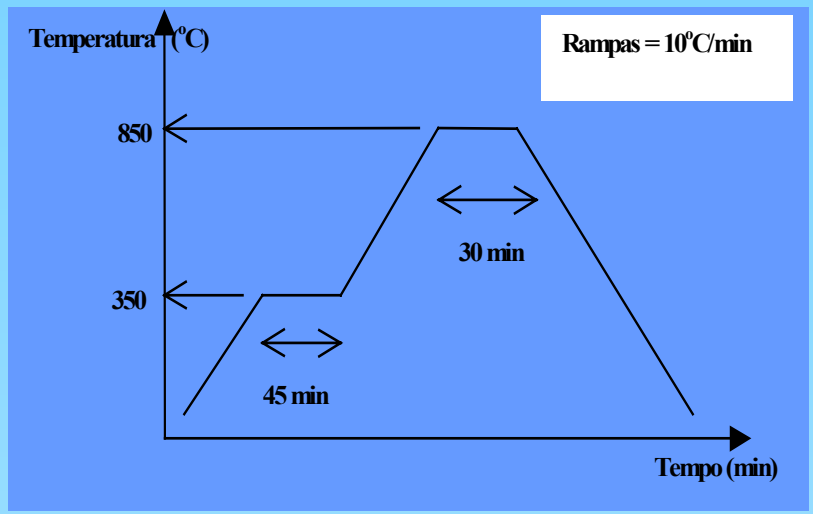
Buried conductors



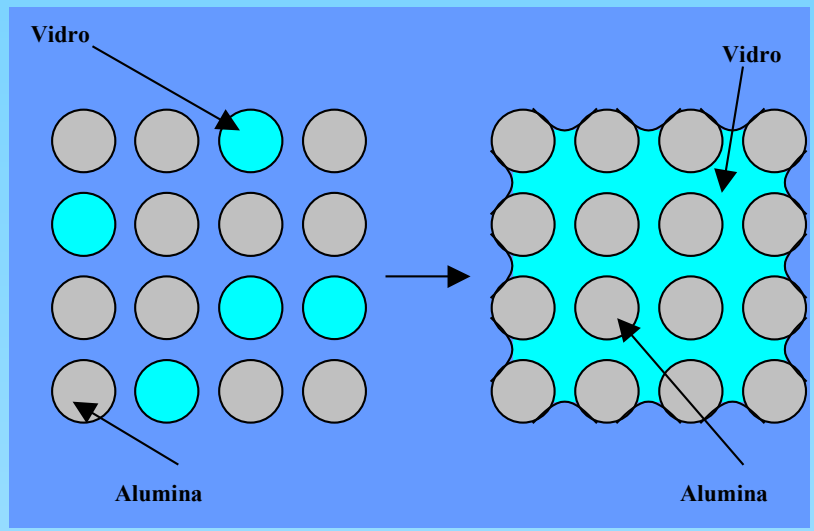
SEM for 3 Layers Face



SINTERING IN LTCC



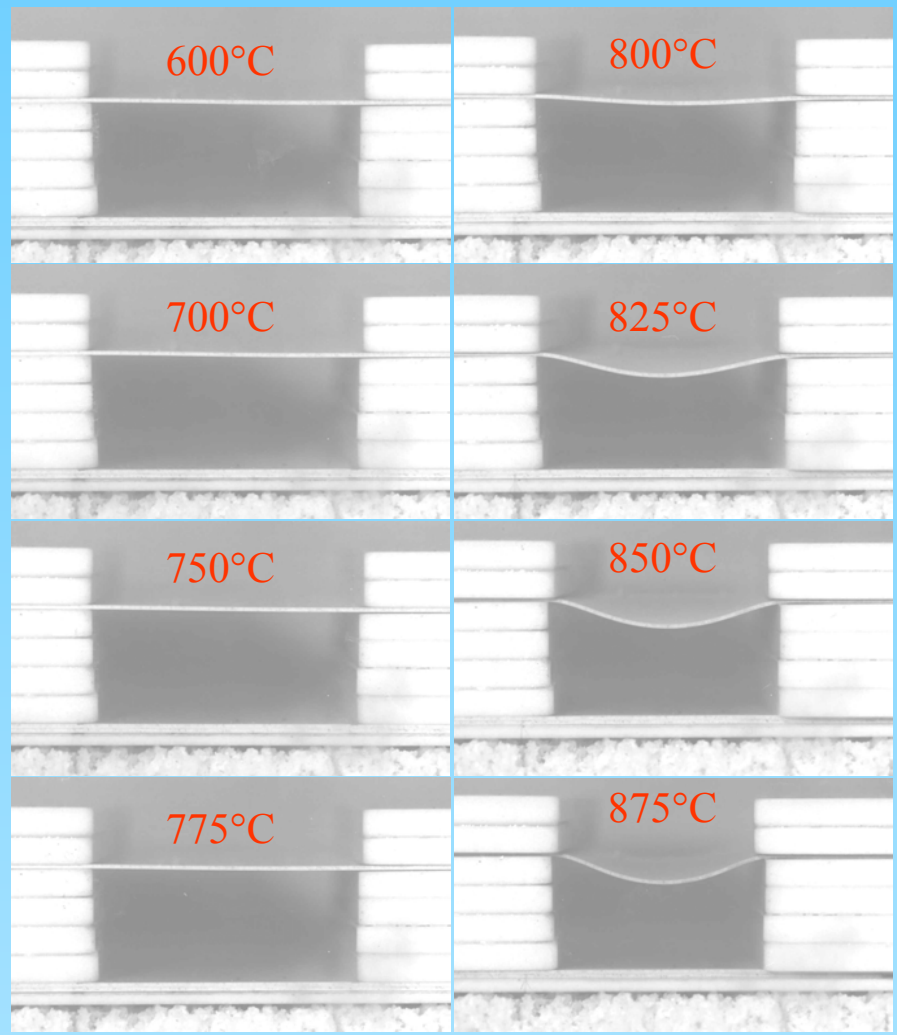
Perfil de temperatura para a sinterização



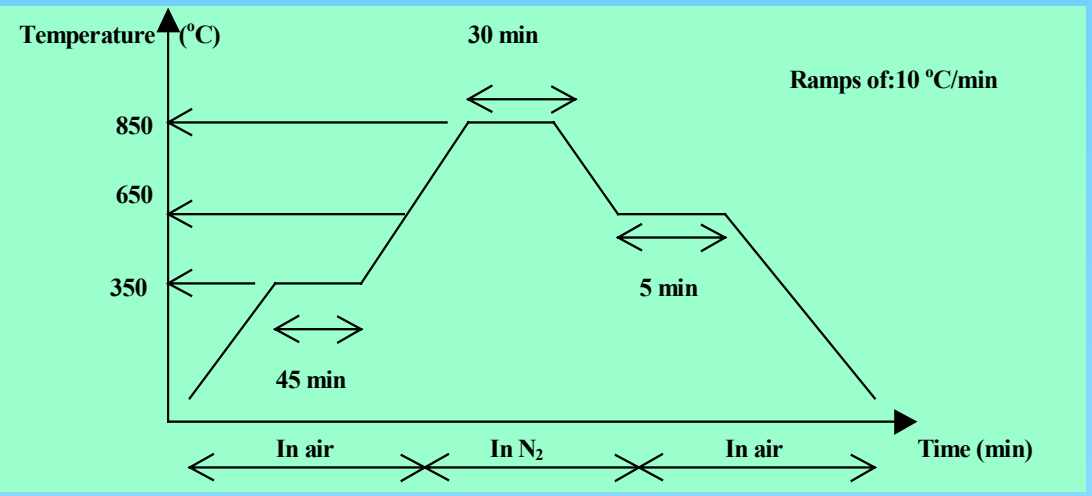
Modelo de sinterização

LTCC TAPES FIRING INDUCED DEFORMATION

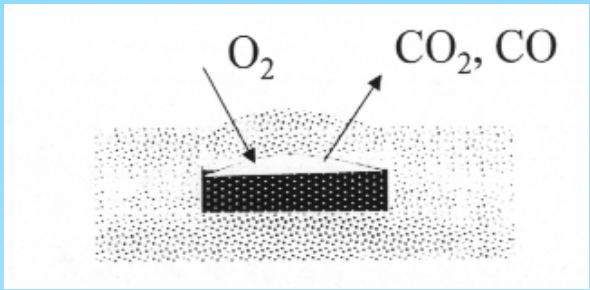
- Firing induced deformation as a function of temperature



COMPENSATION USING FUGITIVE PHASE MATERIALS (GRAPHITE PASTE)

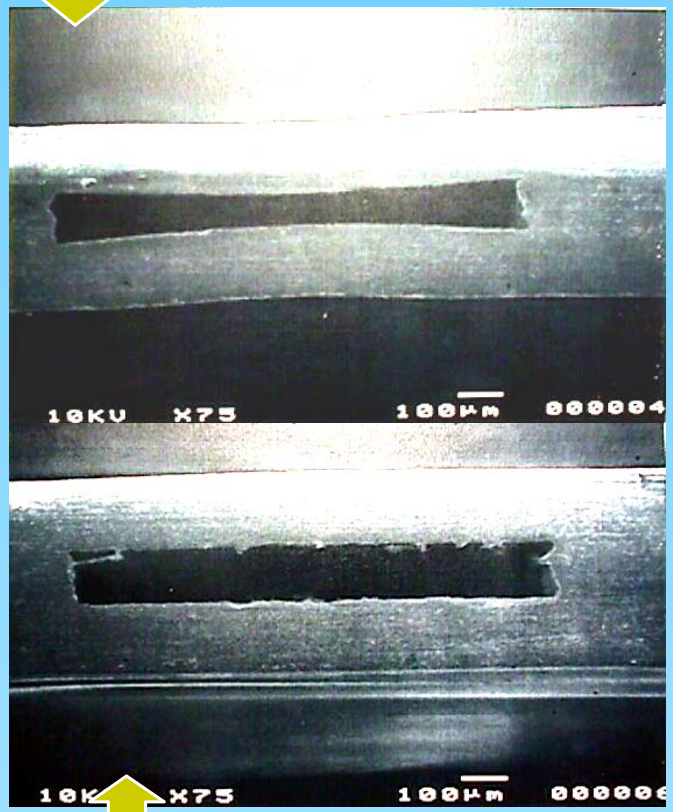


Sintering profile



Sintering Mechanism

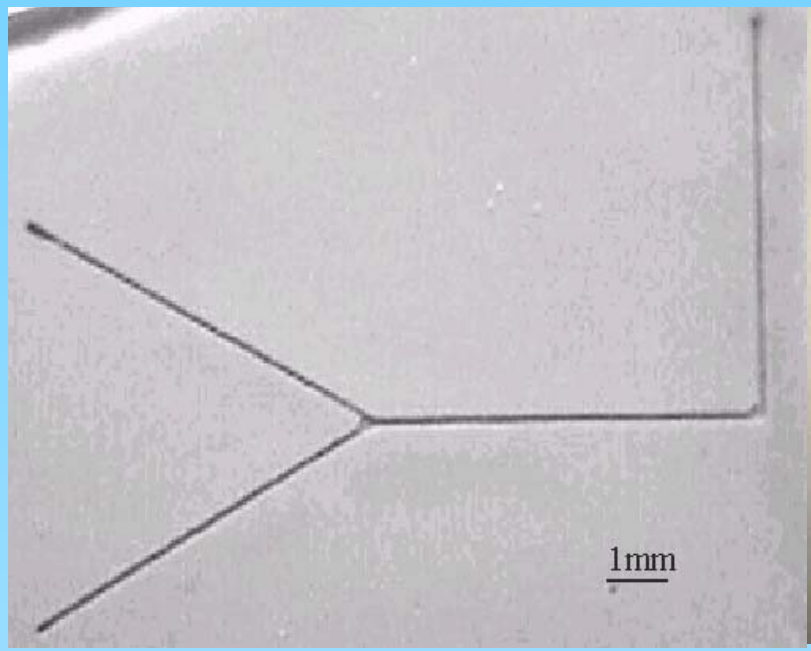
Without graphite



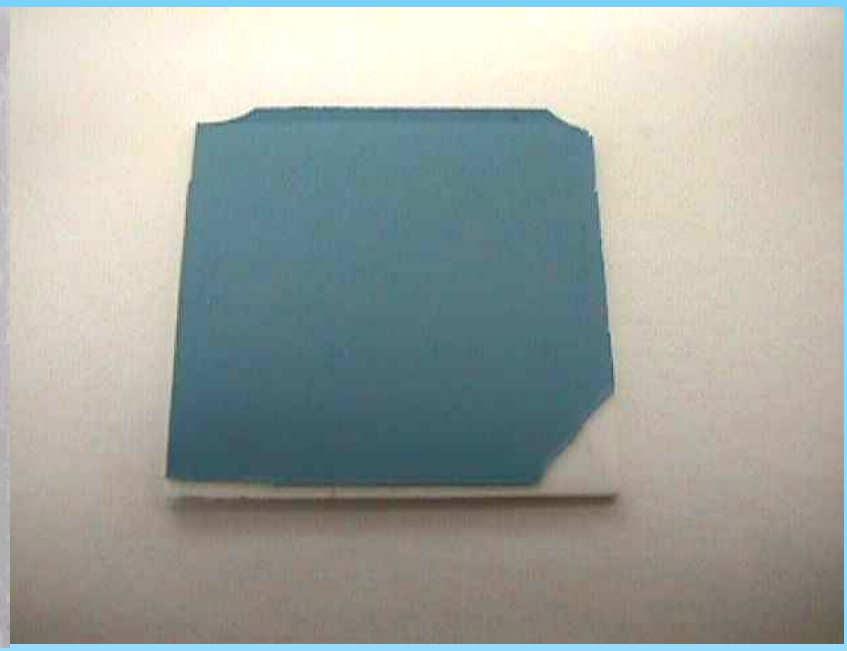
With graphite

BONDING OF LTCC TAPES TO OTHER MATERIALS

LTCC to Glass

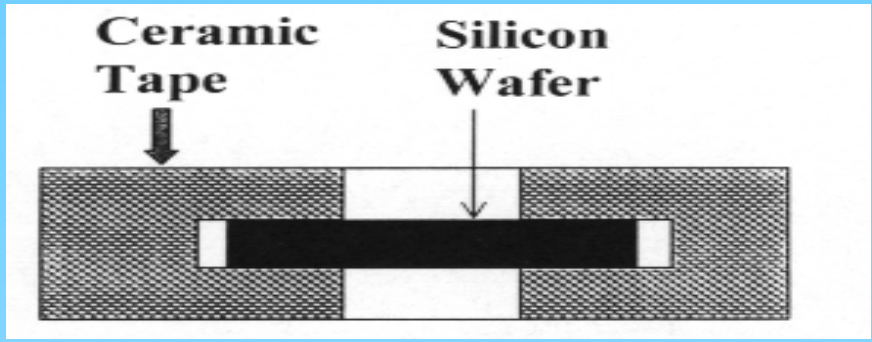


LTCC to Alumina

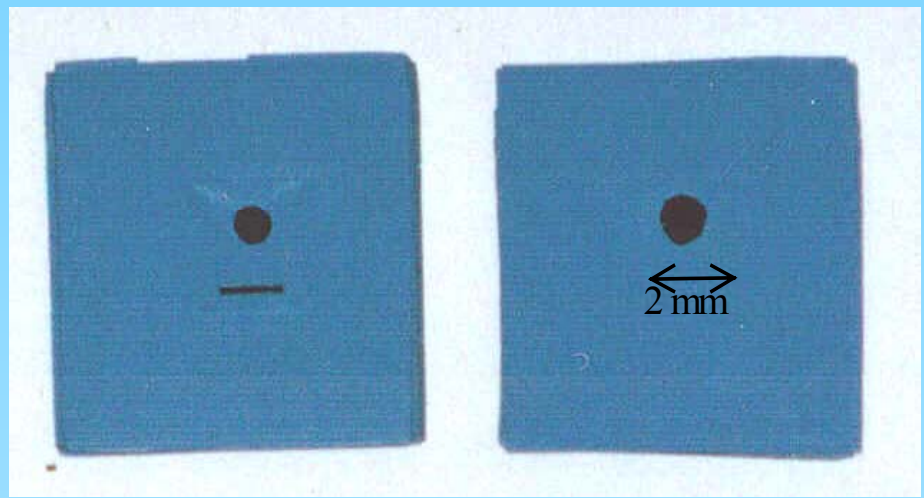


BONDING LTCC TO SILICON

- Silicon can be co-fired or post-fired using metallic die attach pastes or low temperature glazing.

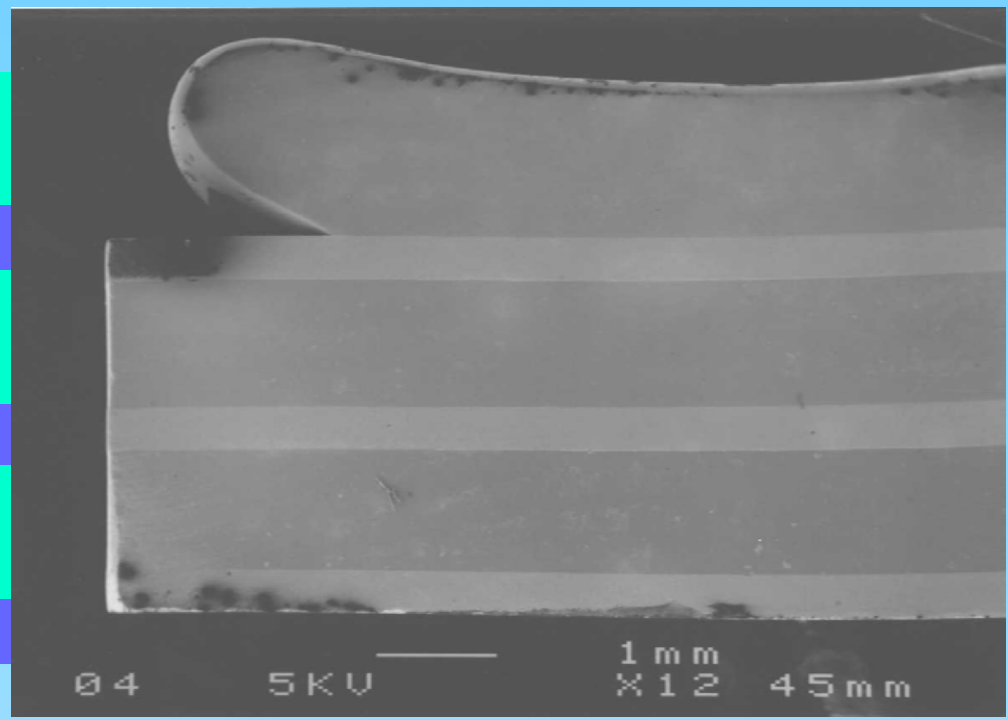


LTCC to Silicon



Silicon in LTCC

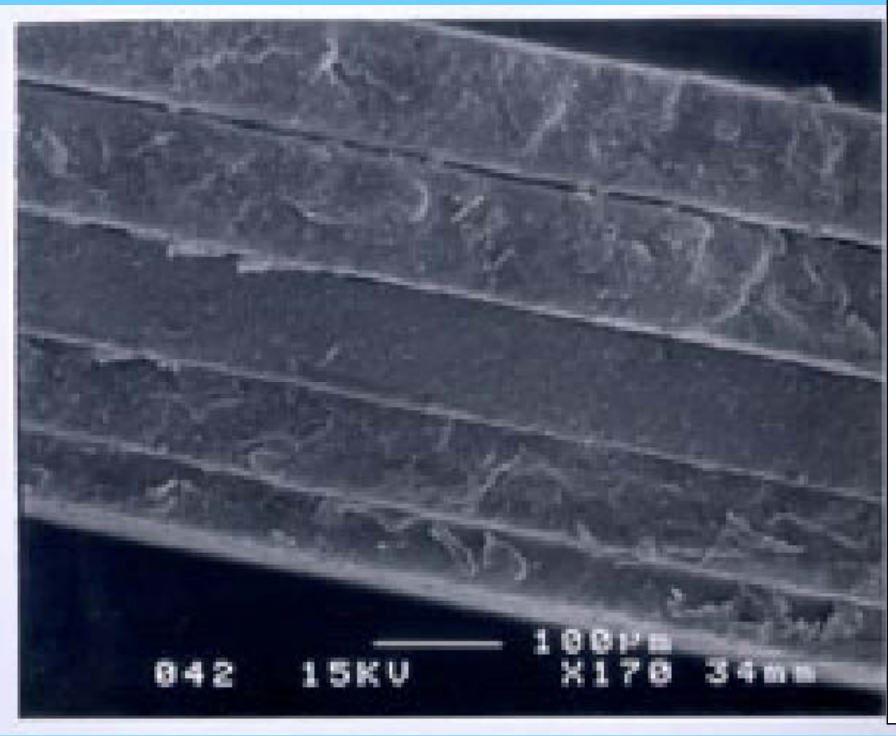
MULTI-LAYERED STRUCTURES WITH GLASS AND CERAMIC TAPES

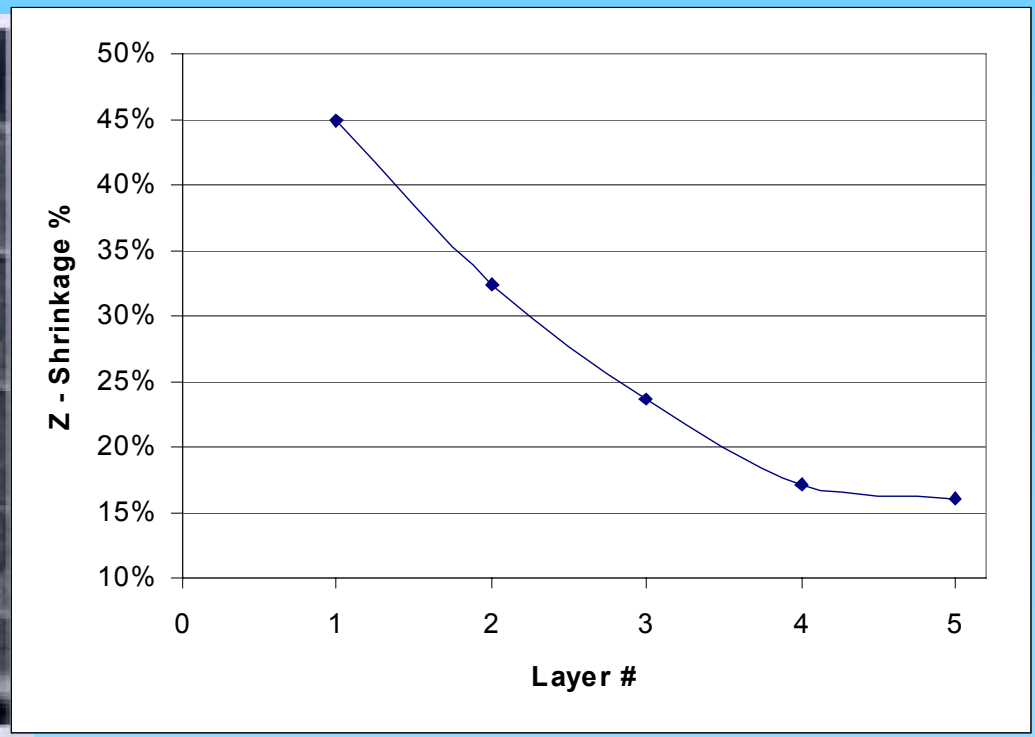


Schematic

SEM of the Sample

CONSTRAINED LAMINATION AND SINTERING

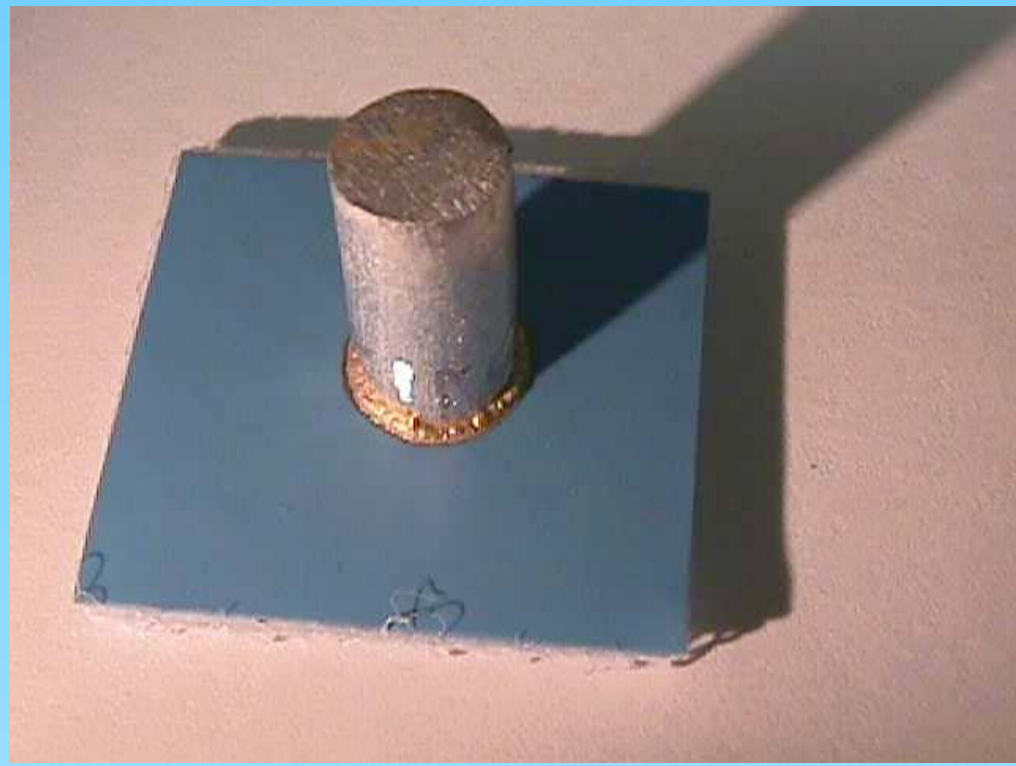




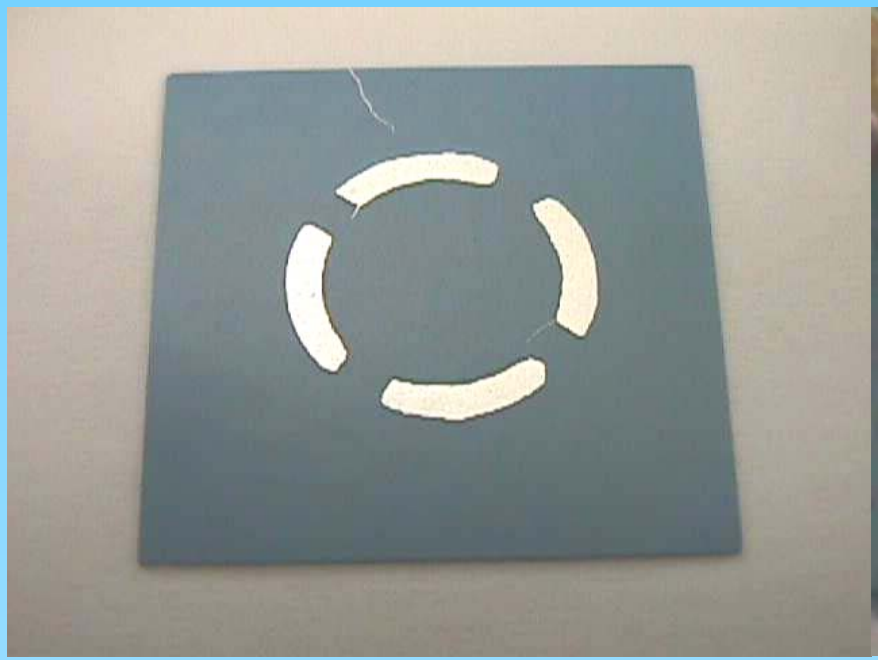
- Z - shrinkage behavior in a multilayer structure under constrained lamination and sintering.

LOW TEMPERATURE BONDING TO LTCC TAPES.

- Devices and subsystems can be attached to LTCC by utilizing low melting point glazes, epoxies, amides and other polymeric adhesives.
- Note an aluminum slug attached to LTCC with Ag loaded epoxy.



THIN AND THICK FILM COMPATIBILITY WITH LTCC TAPES



100 nm Aluminum PVD deposited thin film

15 µm screen-printed piezo- resistor

PHOTO PATTERNED THICK FILM PROCESSES

- Photo Defined Thick Film
- Photo Sensitive Thick Film
- Fodel Compositions
- Diffusion Patterning

PATTERNING ROAD MAP

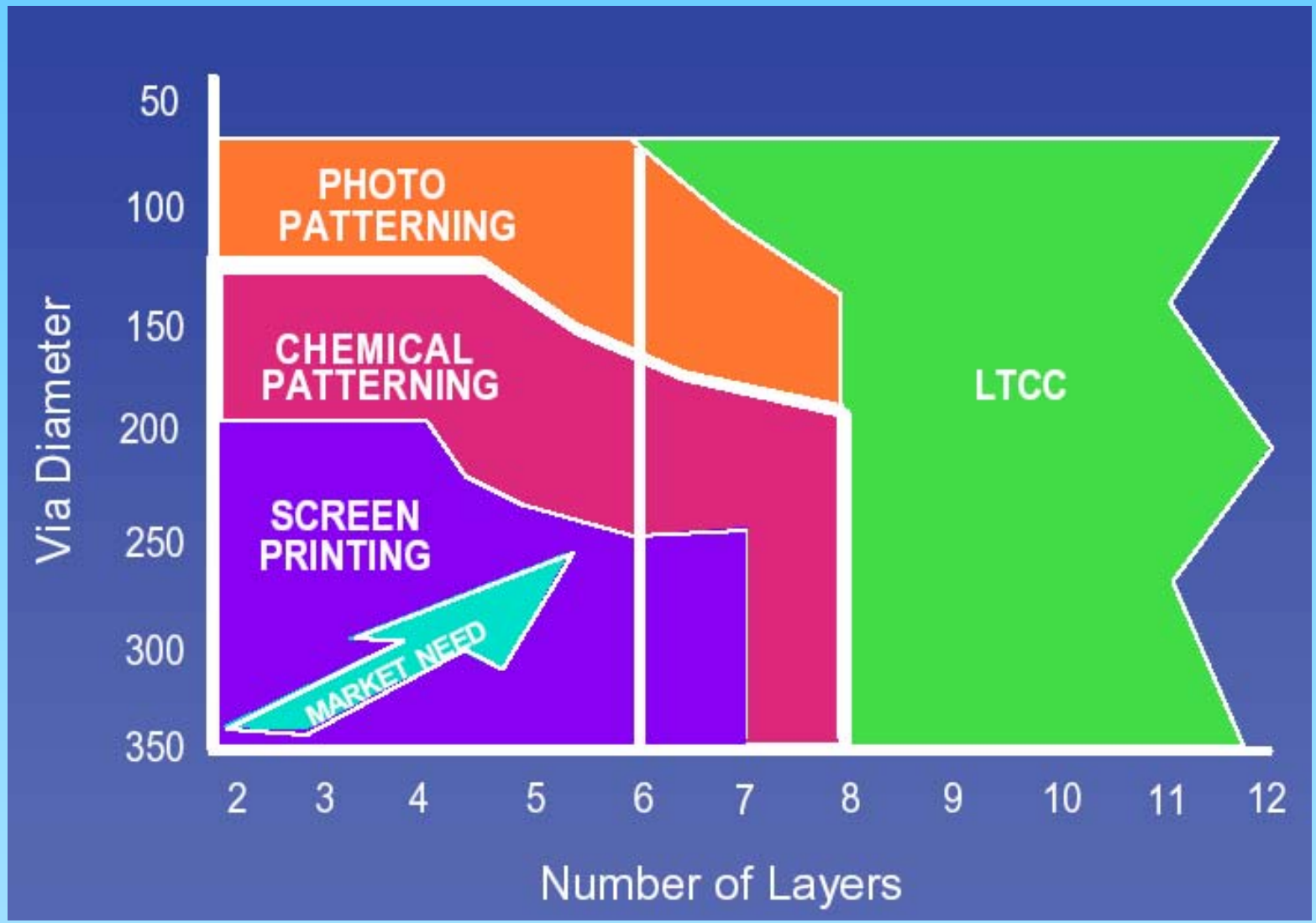


PHOTO THICK FILM TECHNIQUES

- Two main types:-
  - Photodefined – paste (normally conductor) is optimised for etching. Patterned after firing, using a resist, then etched.
  - Photosensitive – paste contains photosensitive material. Patterned by exposing and washing before firing.

PHOTO DEFINED THICK FILM

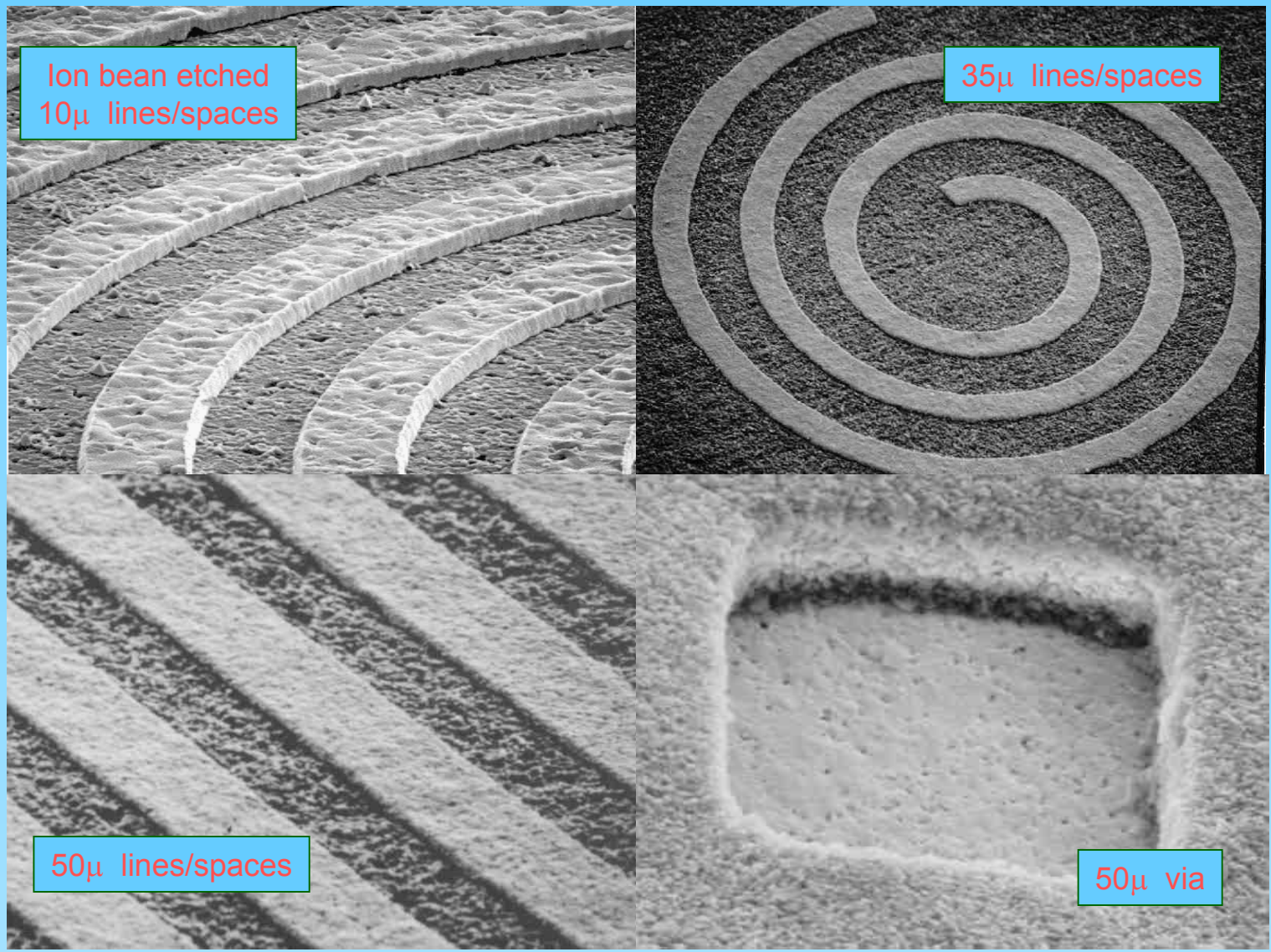
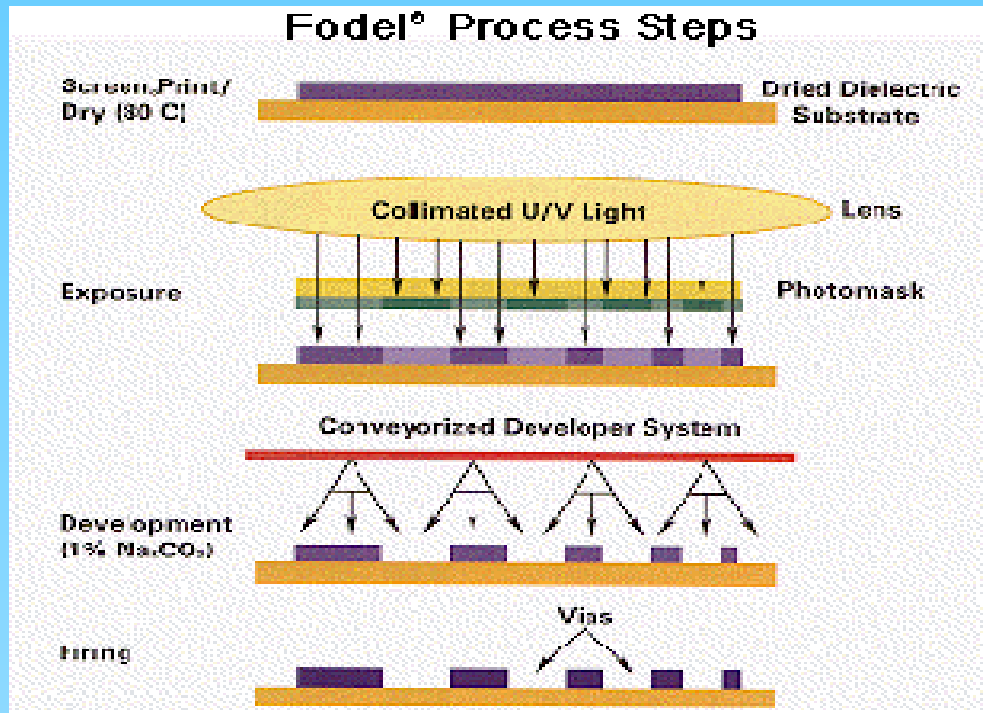


PHOTO SENSITIVE THICK FILM

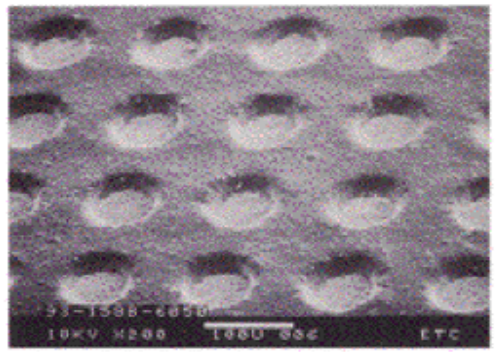
- Thick film on Ceramic, combined with photo-processing
  - **Stability of thick film**
  - **Precision of thin film**
  - **Mass production capability of laminates and IC's**
- High performance conductor & dielectric
  - **Ideal for microwave**

FODEL COMPOSITIONS

- Fodel® materials incorporate photosensitive polymers in the thick film.
- Circuit features are formed using UV light exposure through a photomask and development in an aqueous process.
- Fodel dielectrics can pattern 75 micron vias on a 150 micron pitch, Fodel conductors can pattern 50 micron lines on a 100 micron pitch.
- Fodel materials extend the density capability of the thick film process to allow densities typically achievable using more costly thin film processes.



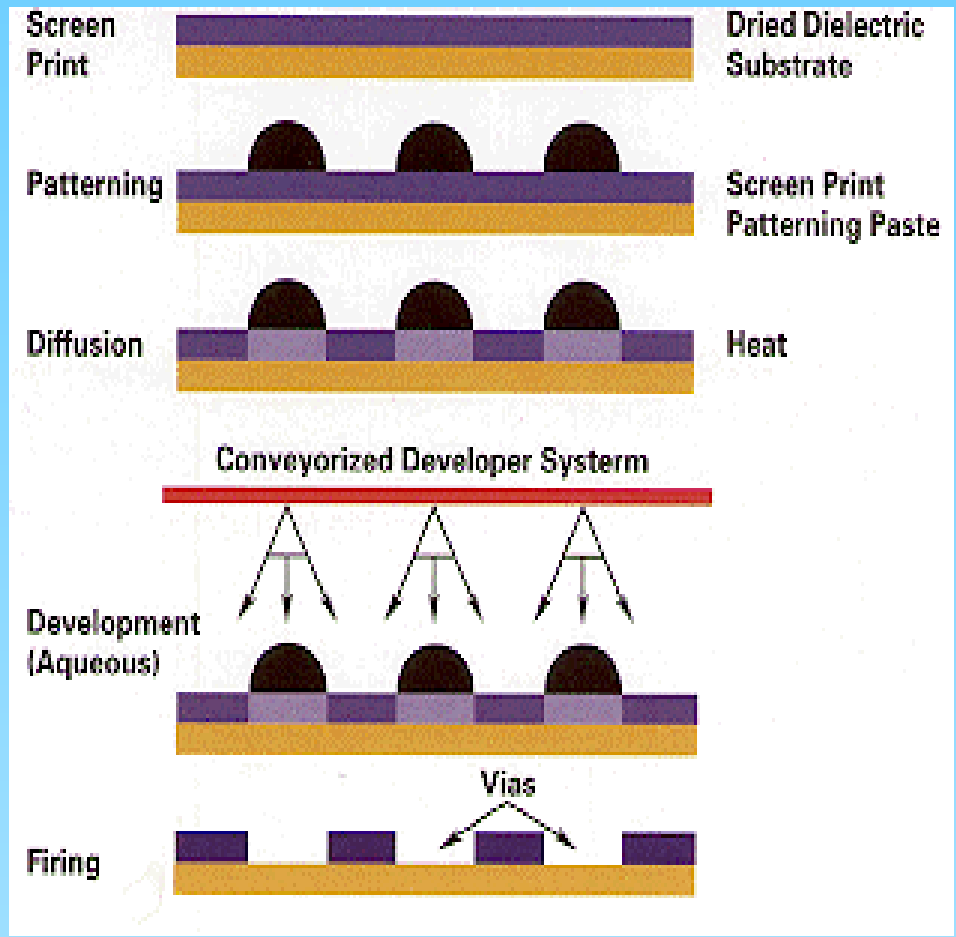
Fodel 6050 Dielectric
75µm (3 mil) Vias



Fodel 5956 Au Conductor
40µm (1.6 mil) Lines

DIFFUSION PATTERNING PROCESS

- The Diffusion Patterning process is based on a chemical reaction between a dried dielectric and an imaging paste which is screen printed on its surface.
- The position of the imaging paste defines the position of the vias.
- The process not only extends the via resolution capability of conventional thick film dielectrics (125 micron vias on a 250 micron pitch have been demonstrated) it does it at much higher yields than the traditional screen printing process can deliver.
- Diffusion Patterning is an environmental friendly aqueous process.
- The process is currently a dielectric imaging process, comparably sized conductor prints are made using advanced screen printing techniques.



NEW LTCC TAPE SYSTEMS

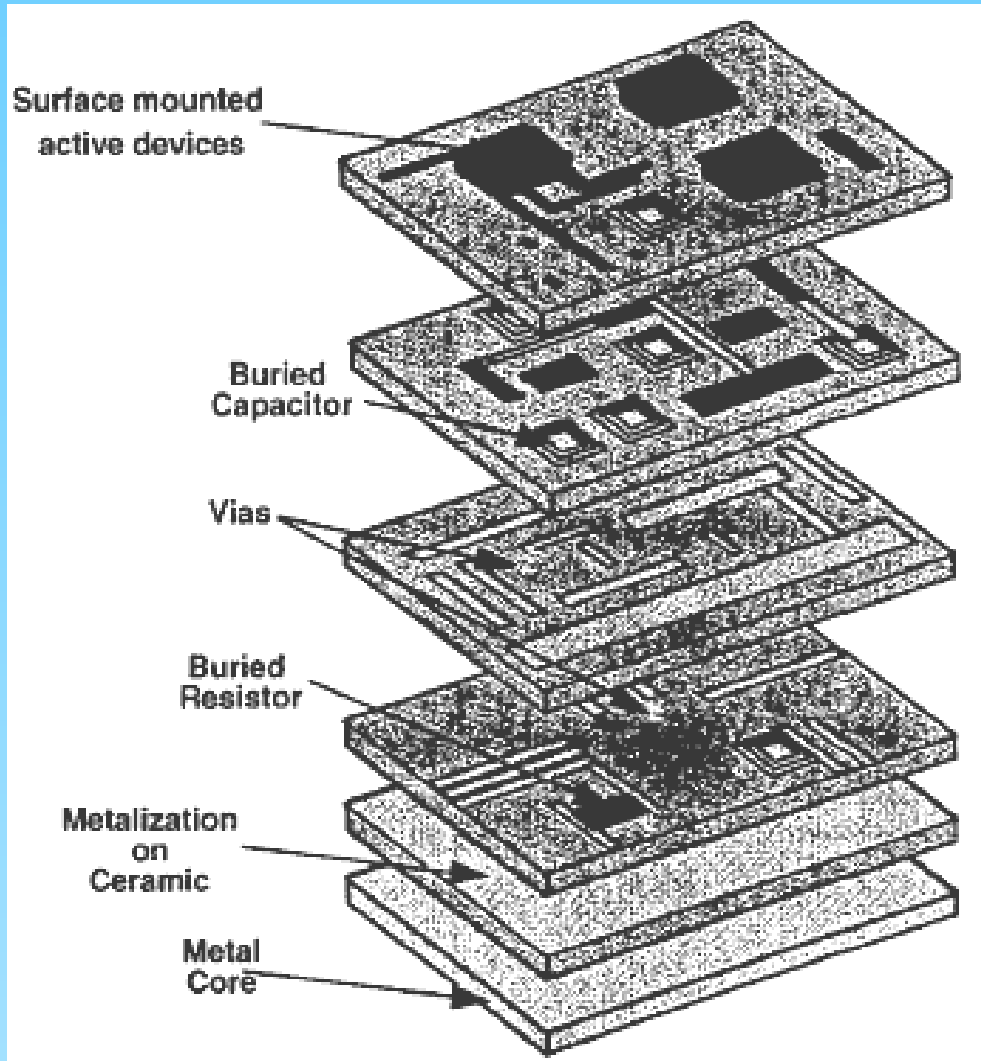
- **Zero Shrinkage LTCC Tapes**
- **LTCC on Metal (LTCC-M)**
- **Transfer LTCC tape (LTCC-C)**
- **Photo Imageable LTCC (PI-LTCC)**

ZERO SHRINKAGE LTCC TAPES

- Recent developments relating to the formulation, processing and manufacturing of ceramic and glass composites, which do not shrink upon co-firing to the degree of ordinary LTCC materials, a slight shrinkage (< 2%) can be controlled to a very tight tolerance of +/- 0.01%.
- Because ZR tapes exhibits a near zero shrinkage and zero shrinkage tolerance upon firing, precise feature locations are maintained in the X, Y, and Z axis's and yield improvements of over 30% can be realized when compared to conventional materials systems.
- Some properties include the embedding and co-firing of: discrete components such as ceramic chip capacitors for true passive integration, ceramic heatspreaders with integral heat pipes for thermal management (>2000 W/mK)
- The main difference between Zero Shrinkage tapes and all other LTCC tapes is its unique shrinkage properties during firing.
- Free sintered this tapes densifies by shrinking in the z-axis.
- Key Benefits are:
  - Near zero (<0.2% ± 0.05%) x-y shrinkage with no added processing steps
  - Compatible with co-fired solderable conductors
  - Cavity structures cut into the green tape show no x-y shrinkage or distortion after firing
  - Lead and cadmium free
  - High Q

LTCC ON METAL (LTCC-M)

- LTCC-M Technology combines conventional LTCC technology with a metal base to provide constrained sintering. Constrained sintering leads to almost zero shrinkage in the x-y plane during the firing process step allowing the accurate placement of embedded components such as resistors, capacitors, transmission lines etc.
- The almost zero x-y shrinkage also leads to ruggedness, improved heat sinks and allows complex cavities with metal ground.



TRANSFER TAPE (LTCC-C)

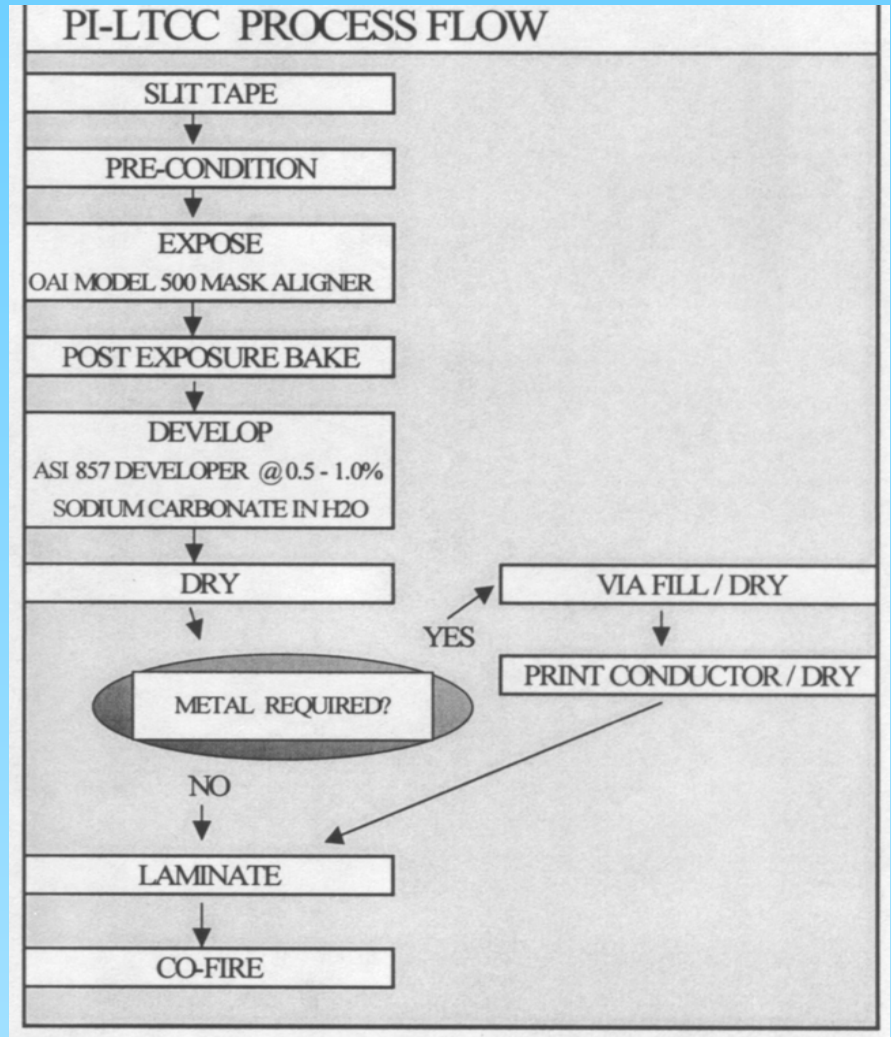
- **A low Dielectric Constant Tape for Use with 96% Alumina Substrates. A flexible cast film of inorganic dielectric powder dispersed in an organic matrix, designed to be laminated to and fired on an Alumina substrate. A pressure/temperature combination of 1.7-6.9 MPa and 70°C works well for laminating this tape.**
- **After lamination, the parts can be fired in a belt furnace at 580°C peak/50 minute cycle burnout followed by an 850°C peak/45 minute cycle for sintering, rendering a fired Shrinkage of : zero to X and Y axis and 45%-55% in Z axis.**
- **Multilayer parts can be formed by metallizing laminated and fired sheets progressively. This tape is useful when low dielectric constant and low loss are desired.**
- **Lo-Fire tape is provided on a silicone-coated polyester film to minimize environmental contamination, to protect it from mechanical damage, and to aid in handling.**

PHOTO IMAGEABLE LTCC (PI-LTCC)

- The PI-LTCC consists of a mixture of photo-polymer organics and ceramic / glass powders doctor bladed onto a 3 mils Mylar film.
- The Photo Imageable LTCC tape offers the advantage of economy by fast and efficient processing combined with the convenience of having an LTCC system very similar in properties to the conventional compositions.

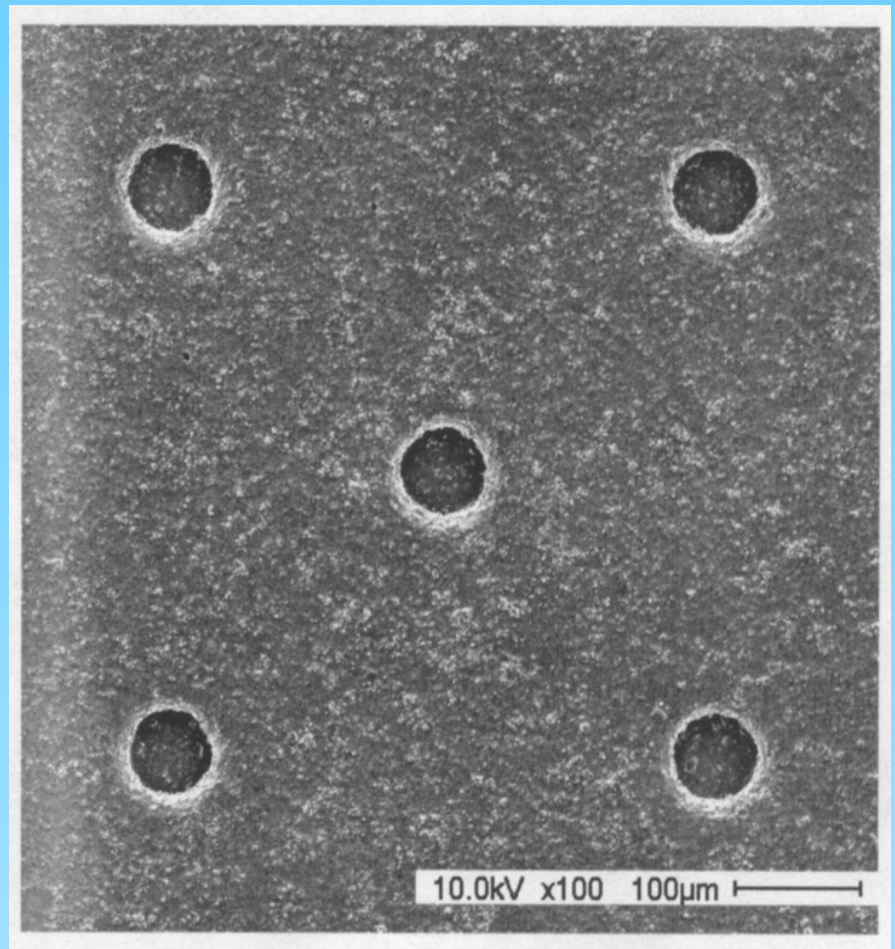
PI-LTCC = LTCC + PHOTORESIST

- UV light (365 nm) passes through a photo mask to expose specific areas of the tape.
- The exposed areas will remain after processing and the unexposed area will be dissolved with a 1% aqueous sodium carbonate solution.
- The rest of the processing is similar to that of the conventional 951 series LTCC tape.



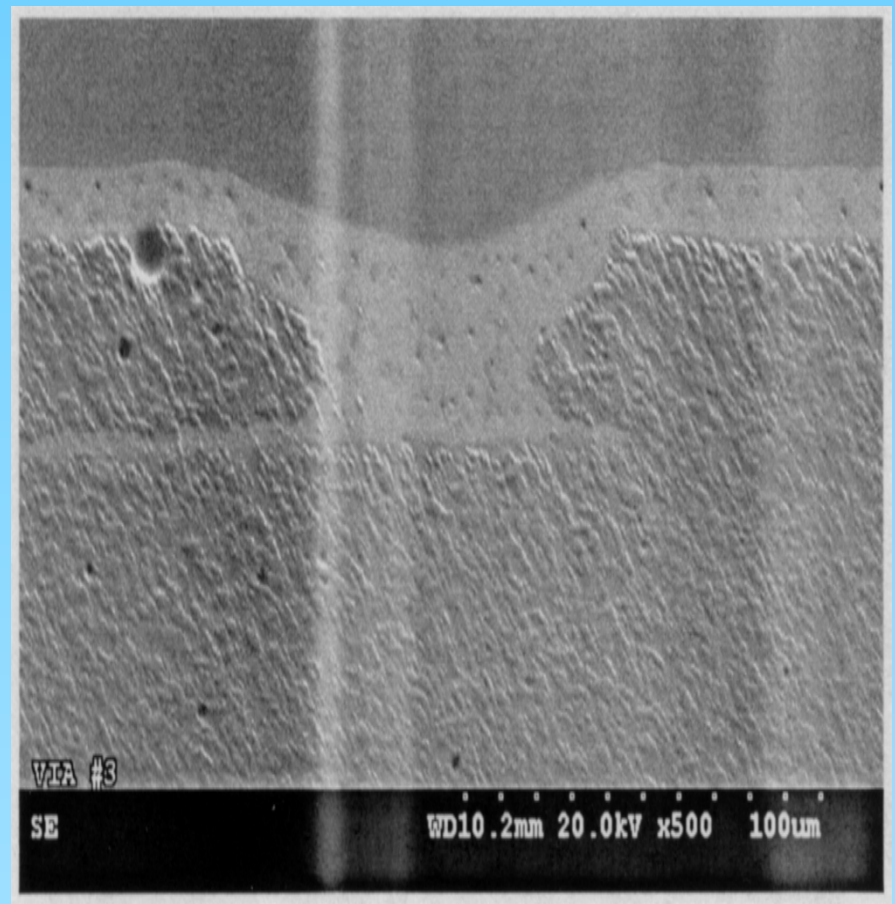
VIAS IN PI-LTCC

- A cluster of vias, 3 mils each with a pitch of 12 mils from a mask containing 18,000 vias (3”X 3” artwork).
- Note that the time required for such a task is dependent only on the tape resolution and the size capacity of the processing equipment.



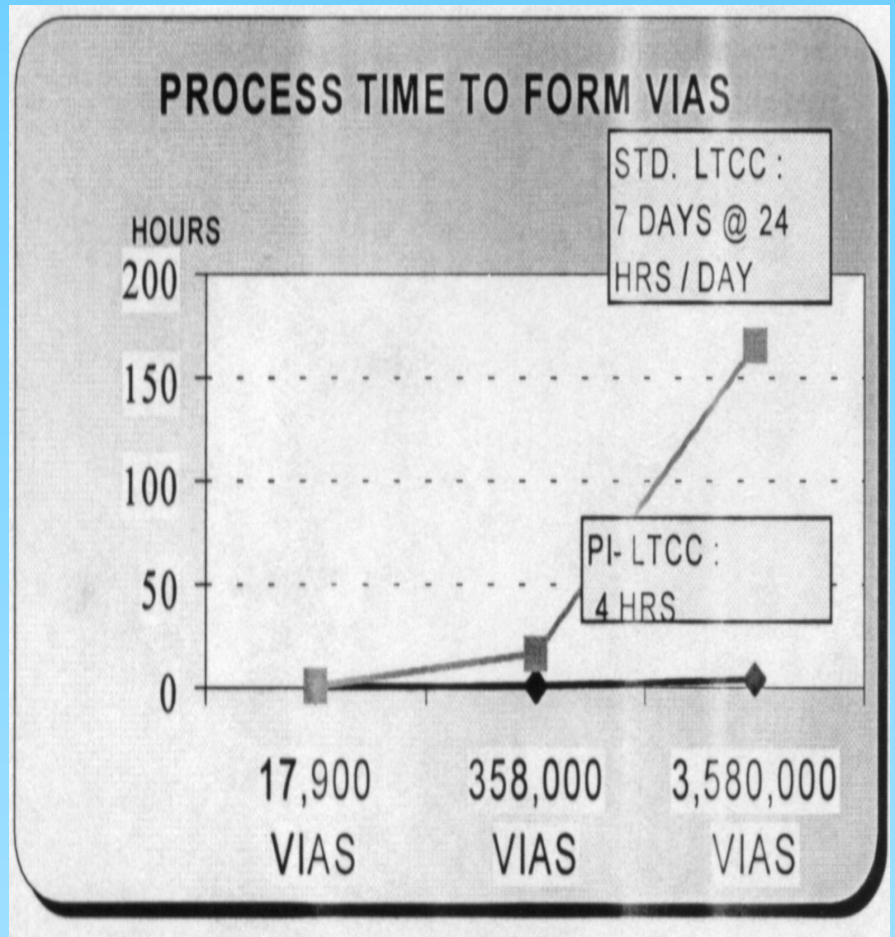
VIA MORPHOLOGY

- A SEM cross section of a typical 3 mils via filled with the 6453 Ag conductor.
- Metallization of the imaged and developed PI-LTCC in the “green” can be done with conventional screen printing thick film conductors or “Fodel” Ag compositions.
- “Fodel” provides efficient means for filling small (less than 5 mils) vias in one process.



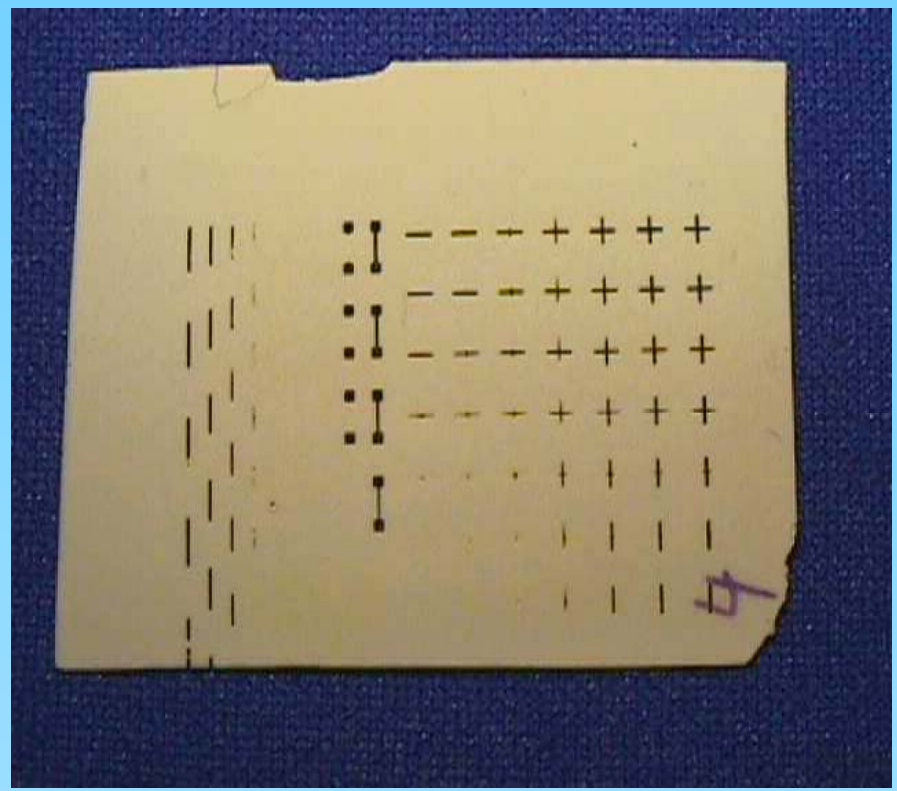
PROCESS TIME TO FORM VIAS

- Remember that the estimated time to punch 3 mils vias (18.000 of them!) using the conventional LTCC is seven days operating the pneumatic puncher 24 hrs a day.
- The same number of vias can be created in just four hours with the photo process.
- The time differential increases non-linearly with the via count.
- Significant savings can be realized in terms of both capital investment and labor cost using PI-LTCC process.



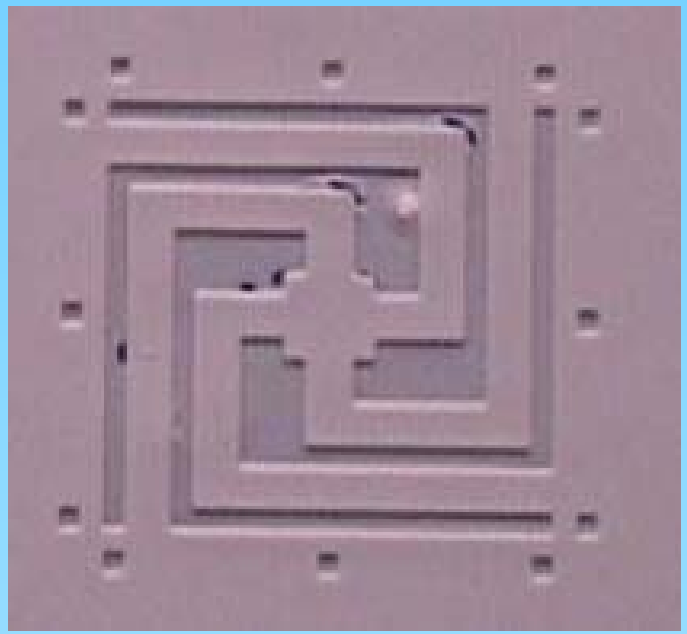
PI-LTCC SPATIAL RESOLUTION EXPERIMENTS

- Test of PI-LTCC tape showing a transferred test pattern.
- The minimum feature size transferred in this photo is 70 microns.
- The process is similar to Si Photolithography.

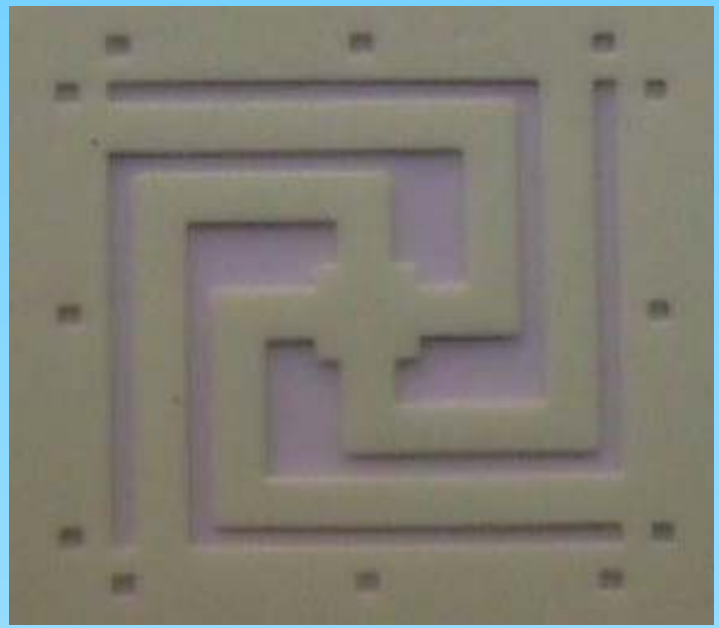


DEVICES USING PHOTO-DEFINABLE CERAMICS

Square Spiral Spring

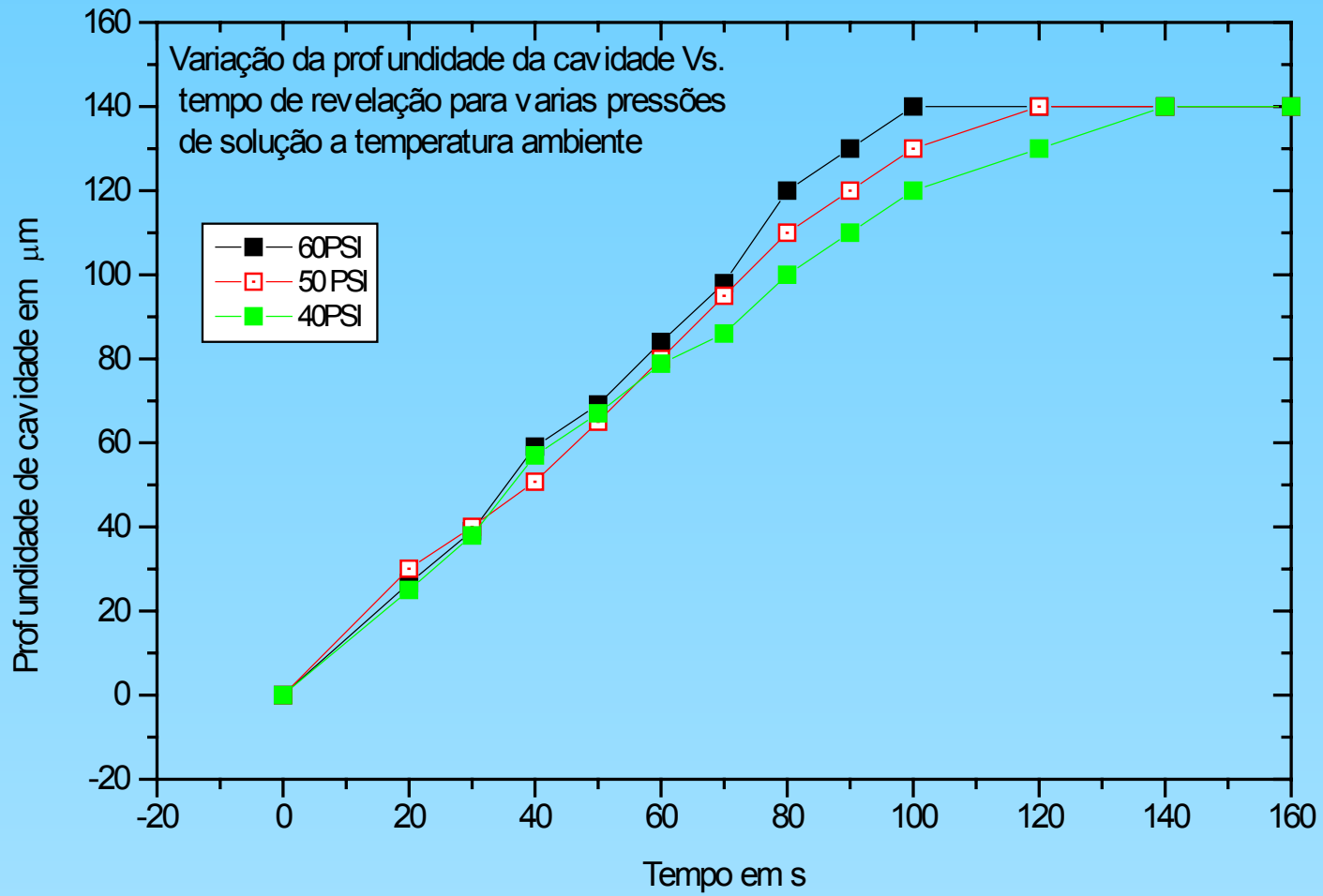


Partial development



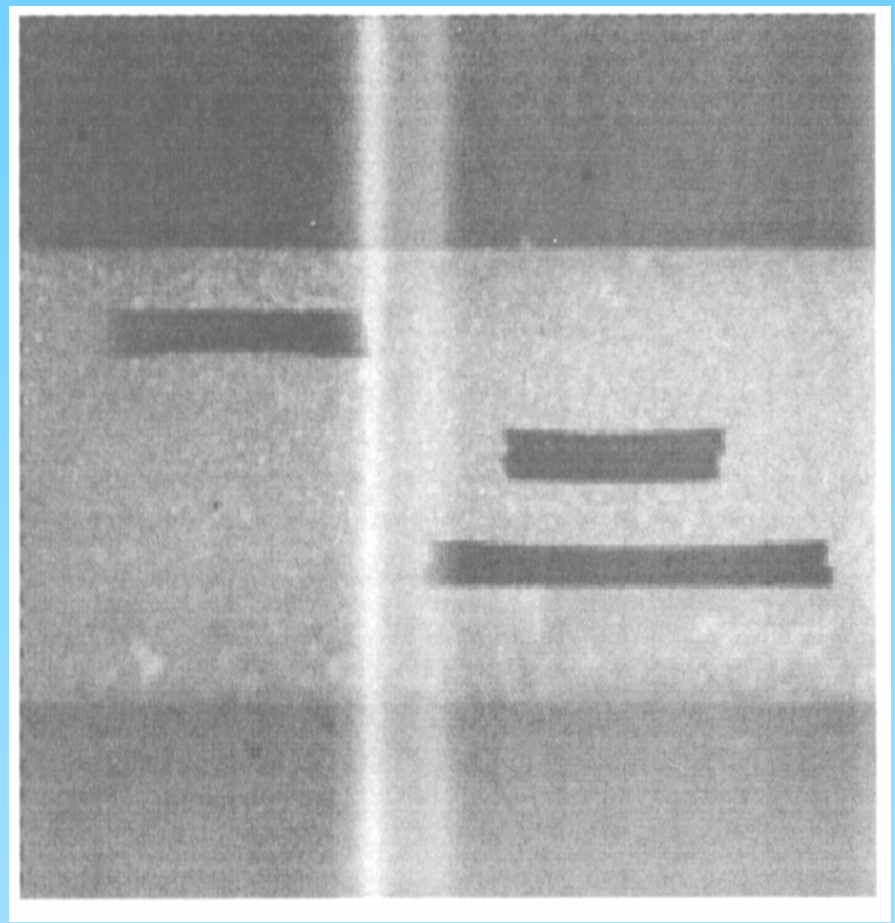
Complete development

PROCESS VARIATIONS OF PHOTO-DEFINABLE MATERIALS



SAGGING IN EMBEDDED CHANNELS

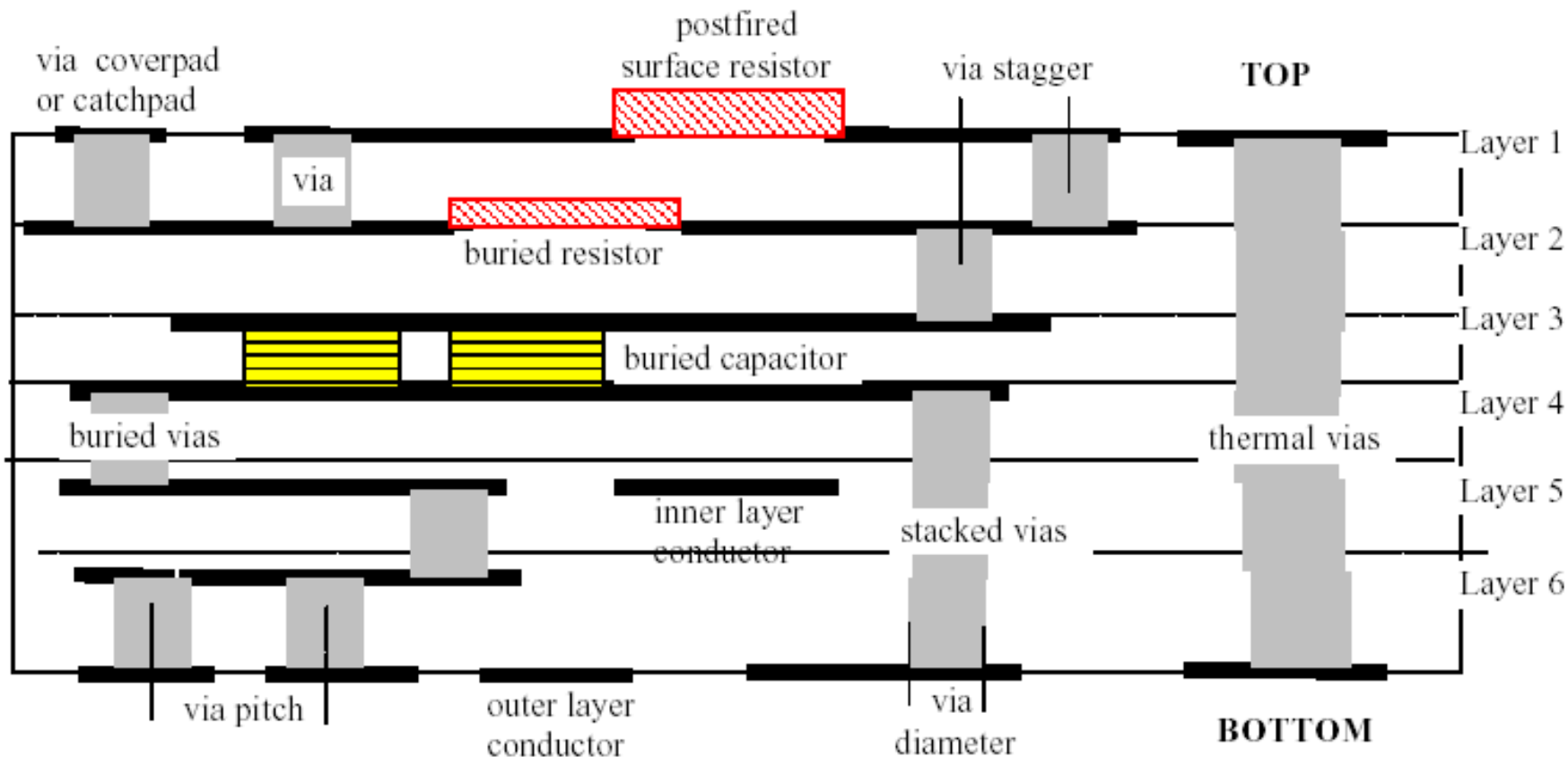
- Three level embedded channels, note a bit of sagging on top of the lower channel in the right of the picture.



LTCC GEOMETRICAL DESIGN RULES

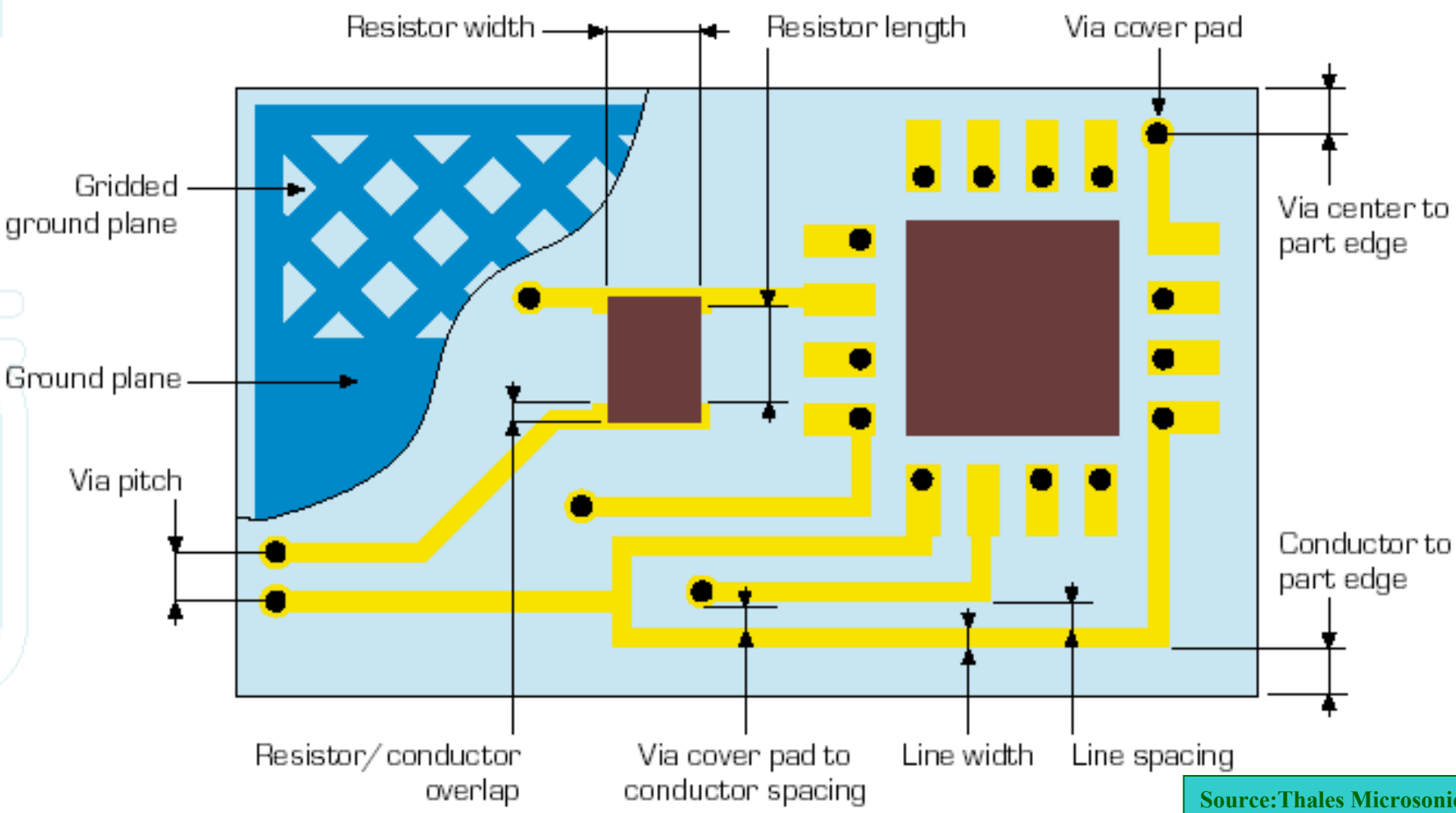
- Conductors
- Vias
- Thermal vias
- Capacitors & Inductors
- Printed resistors
- Cavities / Windows
- I/O

FEATURE LTCC TERMINOLOGY (CROSS SECTION)



Source:Thales Microsonics

FEATURE LTCC TERMINOLOGY (TOP VIEW)



Source:Thales Microsonics

LTCC DESIGN RULES (1) CONDUCTORS

CONDUCTORS

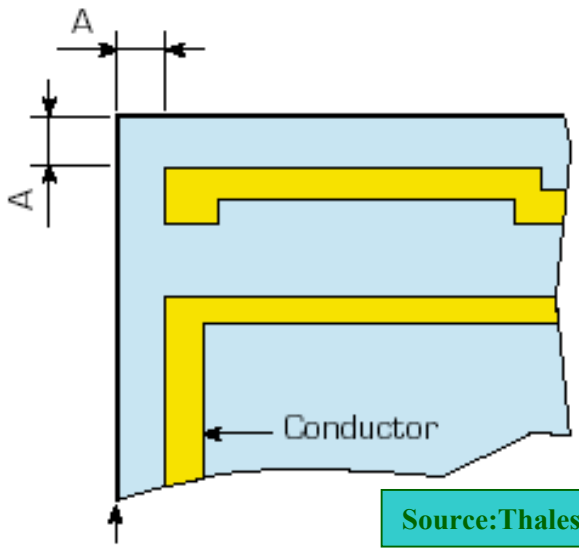
The minimum widths and spacing are defined in the table below.

	Standard	High density
A (µm)	100	75
B (µm)	100	75

Minimum distance between conductors line and vias

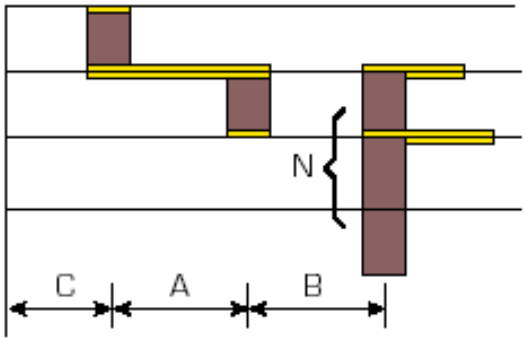
The minimum distance between conductors and edge of the circuit (A) is:

- 150 mm for inner conductors,
- 100 mm for outer conductors.



Source:Thales Microsonics

LTCC DESIGN RULES (2) VIAS



		Standard	High density
Punching ∅ (µm)	951 AX	200	150
	951 P2, PT, C2	150	125
Pitch A (µm)	951 AX	2D = 400	2D = 300
	951 P2, PT, C2	2D = 300	2D = 250
Pitch B (µm)	951 AX	2√2D = 565	2√2D = 425
	951 P2, PT, C2	2√2D = 425	2√2D = 350
Pitch B (µm) for flip-chip	951 PT, C2	2D = 300	2D = 250
Distance to circuit edge C		3D = 450	2D = 250
Max. Qty of stacked vias N		3	10

Source:Thales Microsonics

LTCC DESIGN RULES (3) VIAS

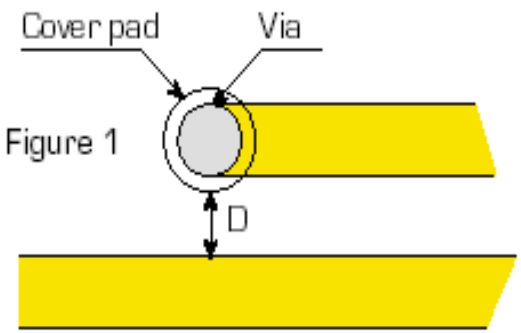


Figure 1

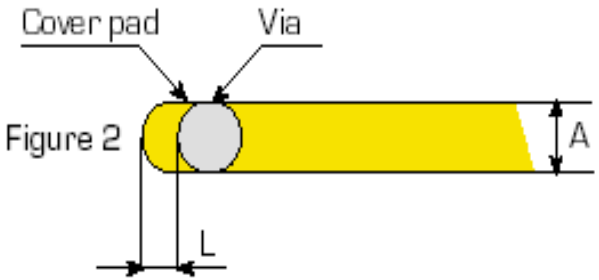


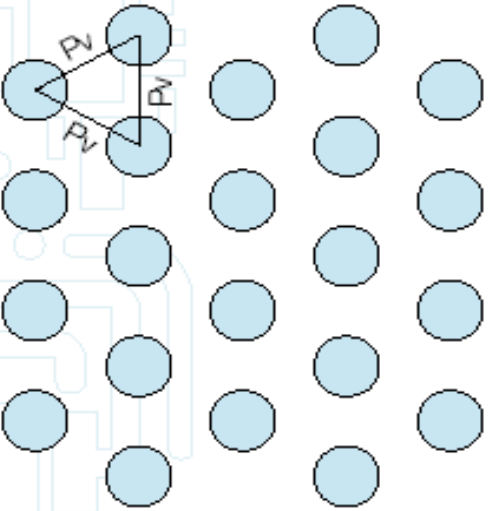
Figure 2

	Standard	High densiity
Ø cover pad co-fired conductors	Ø via + 50 µm	Ø via + 25 µm
Ø cover pad post-fired conductors	Ø via + 200 µm	Ø via + 150 µm
D Distance to conductor	150 µm	125 µm
L co-fired conductors (flip-chip area only)	A / 2	50 µm

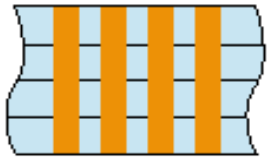
Source:Thales Microsonics

LTCC DESIGN RULES (4) THERMAL VIAS

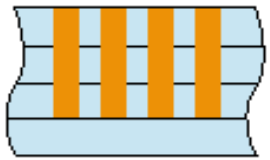
Thermal via distribution

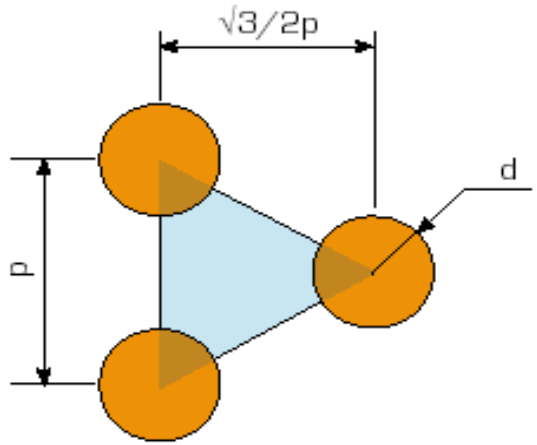


Through thermal via



Blind thermal via for electrical isolation





Source:Thales Microsonics

Via pitch	Via diameter	Via density	Via / diel. area ratio	Equivalent thermal conductivity*
400 µm	200 µm	7.2 via/mm^2	22.7 %	20 W/m/K
600 µm	200 µm	3.2 via/mm^2	10.1 %	8 W/m/K
300 µm	150 µm	7.2 via/mm^2	22.7 %	20 W/m/K
450 µm	150 µm	3.2 via/mm^2	10.1 %	8 W/m/K
		No via		3 W/m/K

LTCC DESIGN RULES (5) CAPACITORS & INDUCTORS

Capacitors

Basic way is to use LTCC tape as a dielectric and conductors planes for electrodes. In these conditions, the capacity value is given by:

$C = \varepsilon A / d$

Where ε is the dielectric constant
A = area of conductive electrodes
d = distance or dielectric thickness

Source: Thales Microsonics

Designation	Value Range	Q Range	Tolerance [1]	ADS Model Availability
Capacitor	0.5 to 20 pF	200 to 90	±7% to ±15% [2]	2001

Inductors

Inductor pattern is shown below. The catch pads, the line width and the distance between lines are based upon general design rules. For yield purpose, it is preferable to locate the catch pad in the center of the coil.

Example for designing an inductor on LTCC

Designation	Value Range	Q Range	Tolerance [1]	ADS Model Availability
Inductor	1 to 60 nH	90 to 30	± 5 % to ± 10 % [2]	Q1 2002

LTCC DESIGN RULES (6) RESISTORS

Calculation of square numbers:

$$N = \frac{R(\text{Ohm}) \times K}{\text{Value of the proposed paste type (Ohm/square)}}$$

For trimmed resistor, calculation is based on Rnominal –30 %

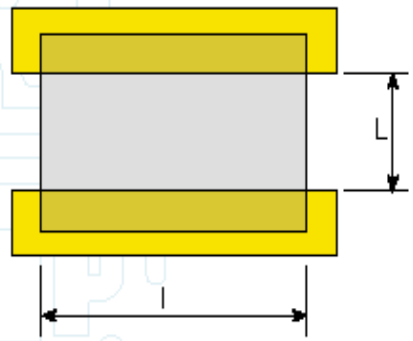
If N > 2 the paste with the upper value is chosen
If N < 0.6 the paste with the lower value is chosen

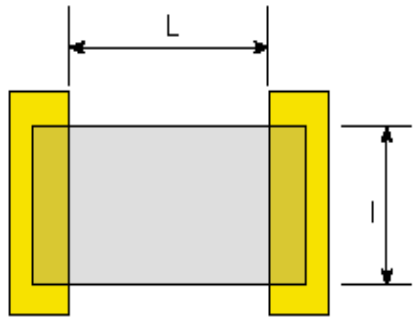
In the critical case, to reduce the number of resistive pastes, it is necessary to have: 0.2 < N < 7.

Calculation of sizes:

$$N = \text{square numbers} = \frac{L}{l} = \frac{\text{Resistor length between electrodes}}{\text{Resistor width}}$$

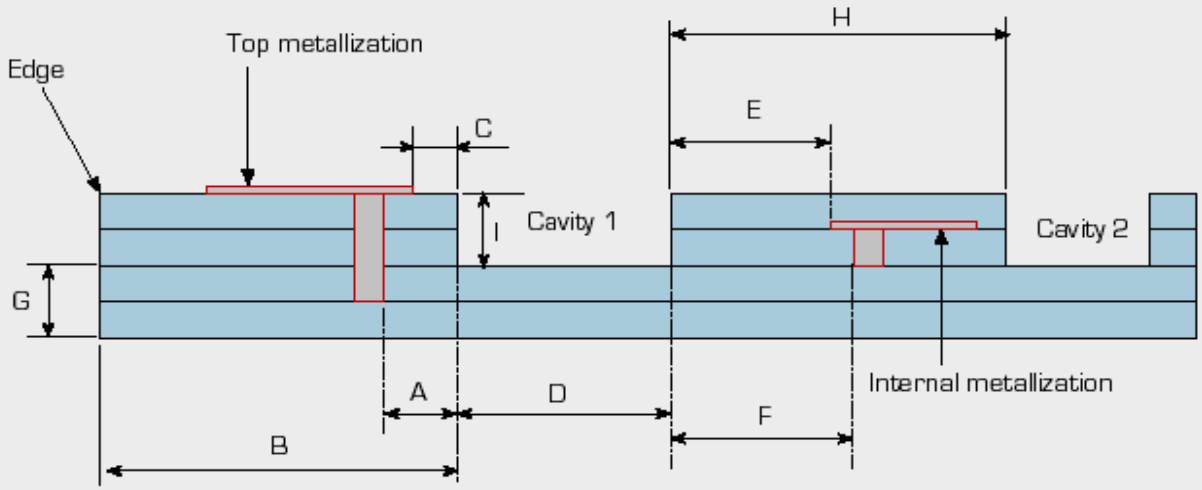
Resistance per square	10 Ω	100 Ω	1 KΩ	10 KΩ	100 KΩ
Corrective factor K	0.9	0.9	1	1.4	2





Source:Thales Microsonics

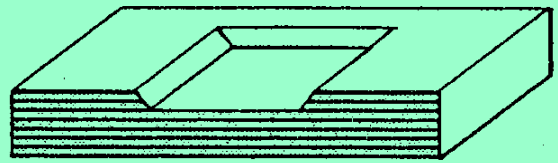
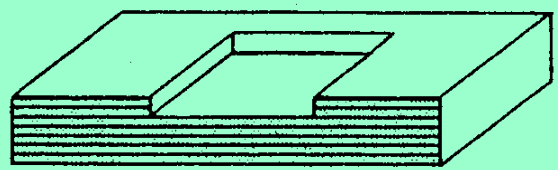
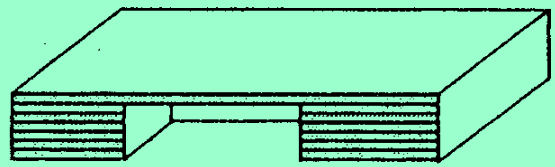
LTCC DESIGN RULES (7) CAVITIES



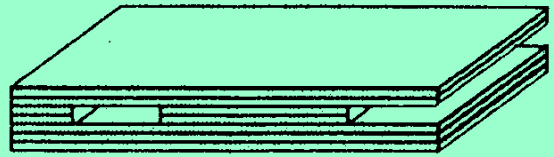
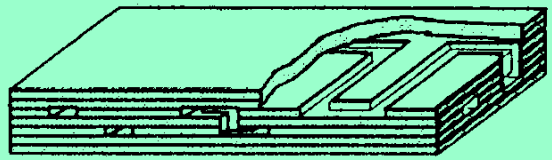
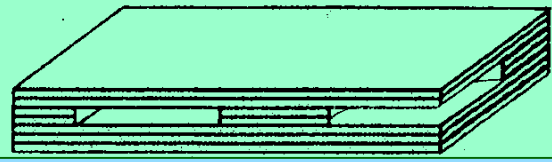
Source:Thales Microsonics

Distance of cavity edge to a via not connected to any internal conductor close to the cavity edge	A	≥ 250 µm
Distance of cavity edge to the edge of the substrate	B	≥ 1500 µm
Distance of cavity edge to end of top metal layer	C	≥ 150 µm
Maximum size of a cavity m	D	max: area of 20 x 20 mm
Distance of cavity edge to end of internal metal layer or conductor line	E	≥ 250 µm
Distance of cavity edge to a via connected to an internal conductor line	F	≥ 275 µm
Minimum thickness under the cavity	G	370 µm minimum [1]
Cavity to cavity spacing	H	≥ 1500 µm
Cavity height	I	< 2 x H

TOP LAYER CAVITIES IN LTCC TECHNOLOGY

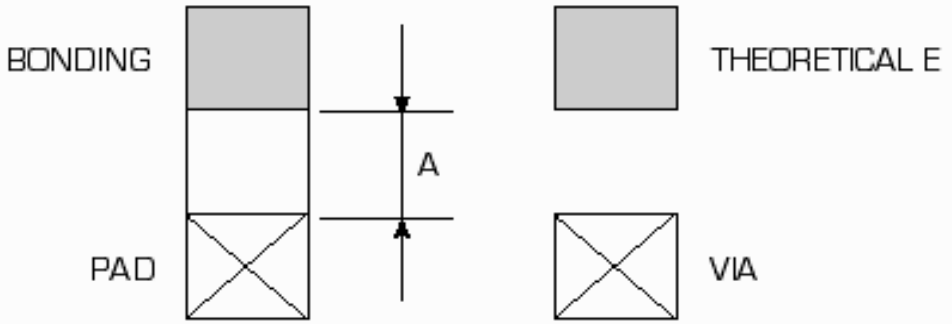
Cavity requirements	Application examples	View of set-up
no special requirements	sensor carrier actuator carrier gas sensor	
high edge quality	sensor carrier pressure sensor dies for innerlayer cavities	
thin membran under /over cavity	pressure sensor	

INNER LAYER CAVITIES IN LTCC TECHNOLOGY

Cavity requirements	Application examples	View of set-up
simple through holes (x- or y-direction)	flow sensor cooling functions	
small capillary tubes capillary systems	chemical sensor cooling systems microfluidic systems	
expanded innerlayer cavities	pressure sensor chemical sensor	

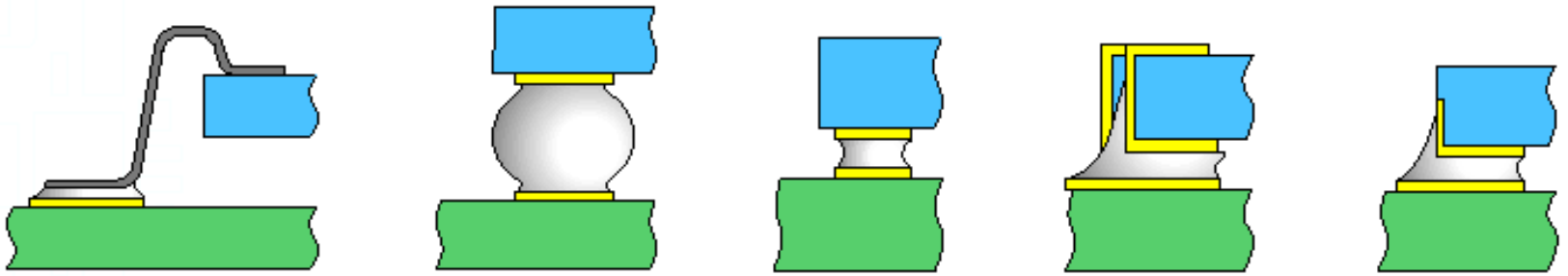
LTCC DESIGN RULES (8) WIRE BONDING & I/O STYLES

Dimensions of the die bonding pad must be 20 mils larger than the maximum sizes of the die, (10 mils in the case of dense layouts).
Insulation between pads must be 5 mils minimum.



A: Distance between the edge of the bonding area and the edge of the via:

- standard = 10 mils
- minimum = 5 mils

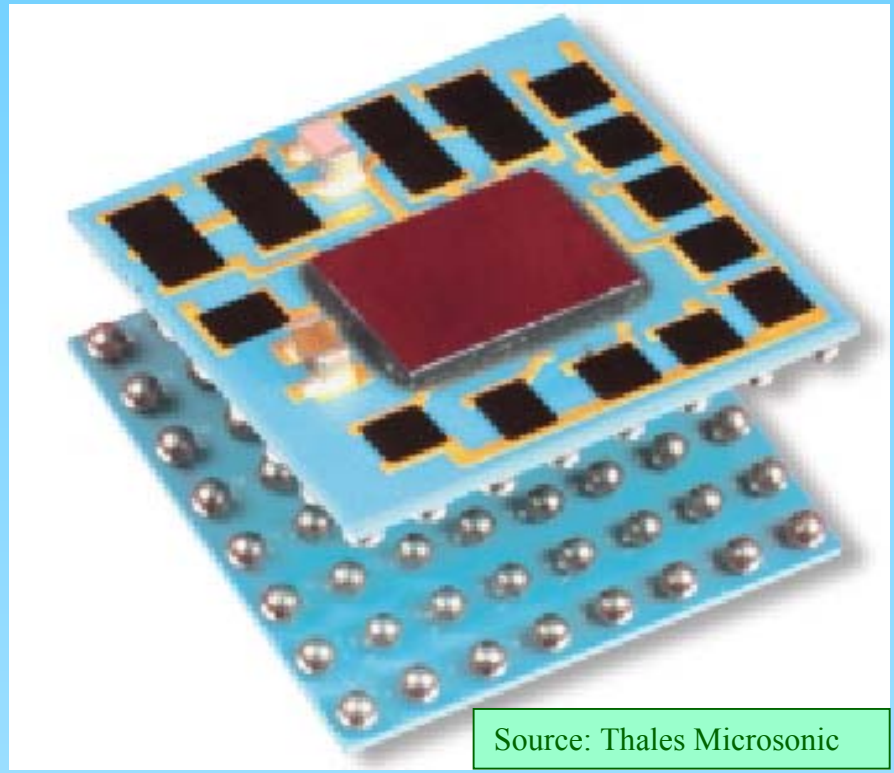


Source:Thales Microsonics

LTCC ADVANCED PACKAGING TECHNIQUES

- Low Temperature Cofired Ceramic technology (LTCC) is adapted to high performance assembly and packaging techniques like flip-chip and BGA.
- The combination of this 3 technologies allows the design and fabrication of very high density and cost effective Single Chip and Multi Chip Modules.

- Flip Chip BGA CSP



Source: Thales Microsonic

FLIP-CHIP ON LTCC

- Characteristics of flip-chip on LTCC
  - **Peripheral and area I/O pad distribution**
  - **I/O pitch down to 250 µm (125 µm bump)**
  - **3 possible bonding techniques**
    - **SnPb solder reflow**
    - **thermocompression**
    - **conductive adhesive**

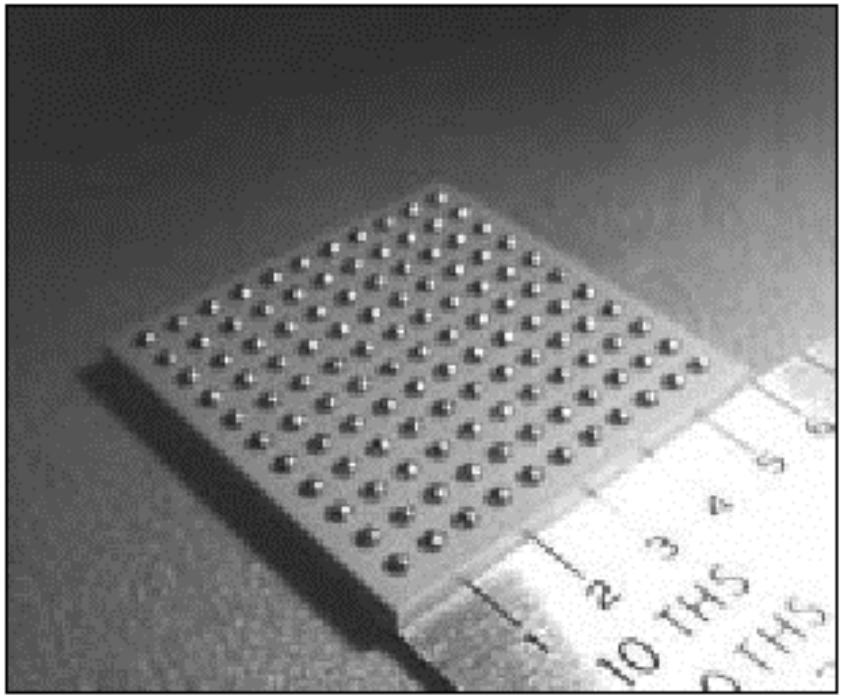
- Advantages of flip-chip on LTCC
  - **Direct bonding on top vias (no additional metallization required)**
  - **LTCC CTE very close to silicon CTE**
  - **High routing capability of the LTCC technology thanks to:**
    - **buried via structures (diameter down to 100 µm)**
    - **line pitch down to 200 µm**
    - **high number of layers**

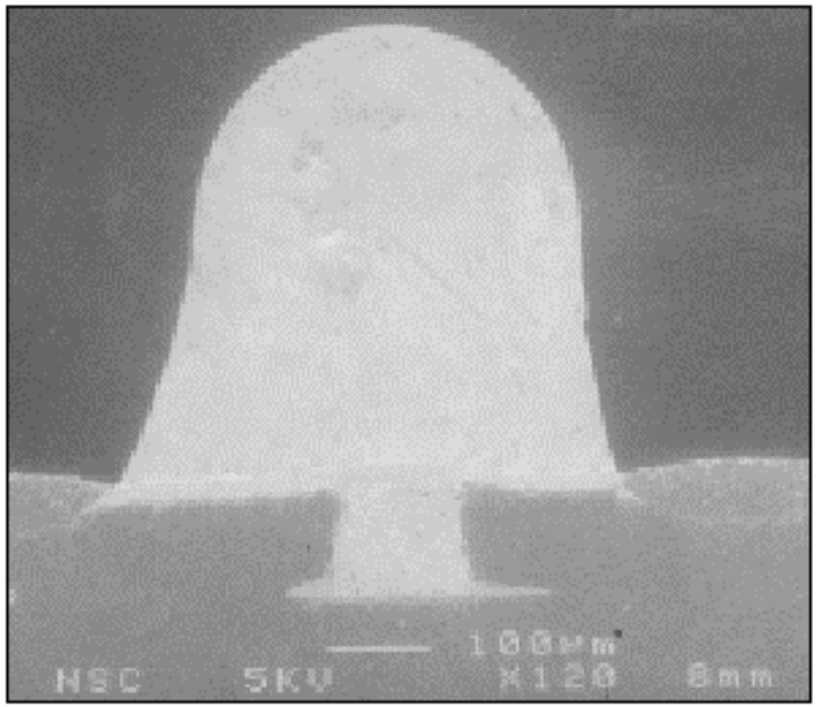
BALL GRID ARRAY WITH LTCC

- Characteristics of BGA with LTCC
  - **Ball pitch from 0.75 mm to 1.5 mm**
  - **Body size from 5 x 5 mm2 to 40 x 40 mm2**
  - **Number of I/Os up to 961**
  - **High temperature solder balls**
  - **Adapted to single and multi-chip module design**
  - **Large range of techniques for die protection**
    - **Glued metallic or ceramic lid**
    - **Epoxy overmolding or glob top**
    - **Brazed hermetic Kovar ring**
- Advantages of BGA with LTCC
  - **High design flexibility**
  - **Very high number of I/Os at reasonable pitch**
  - **High routing capability of the LTCC**

LTCC-BGA

Part and Cross Section – 30 mil ball





Source: National Semiconductors

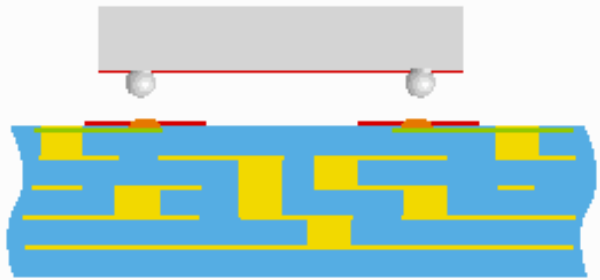
LTCC DESIGN RULES (9) FLIP-CHIP

FLIP CHIP ASSEMBLY

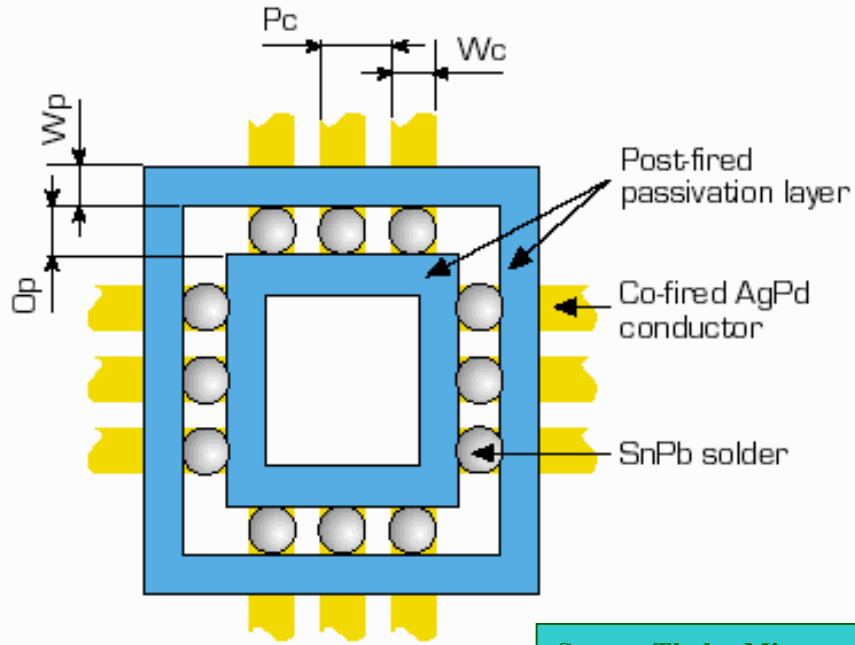
Flip Chip on co-fired AgPd conductor pads using solder reflow.

Parameter	Symbol	Value
AgPd pad width	Wc	150 µm min.
AgPd pad pitch	Pc	250 µm min.
Passivation opening	Op	150 µm min.
Passivation width	Wp	200 µm min.

Figure 1: Flip chip assembly

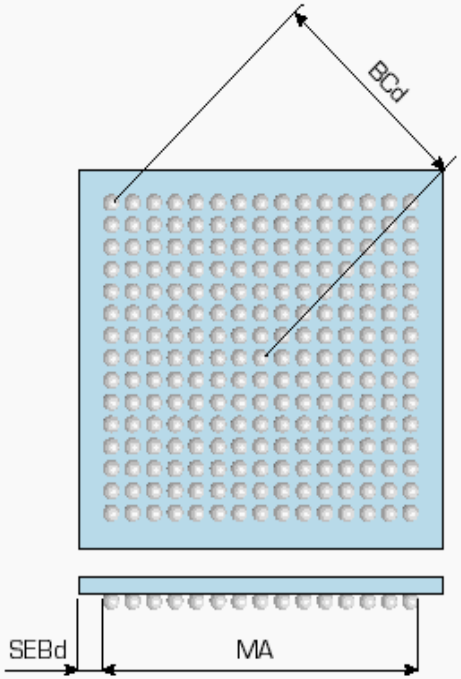


Flip Chip Assembly on LTCC Structures for solder reflow techniques

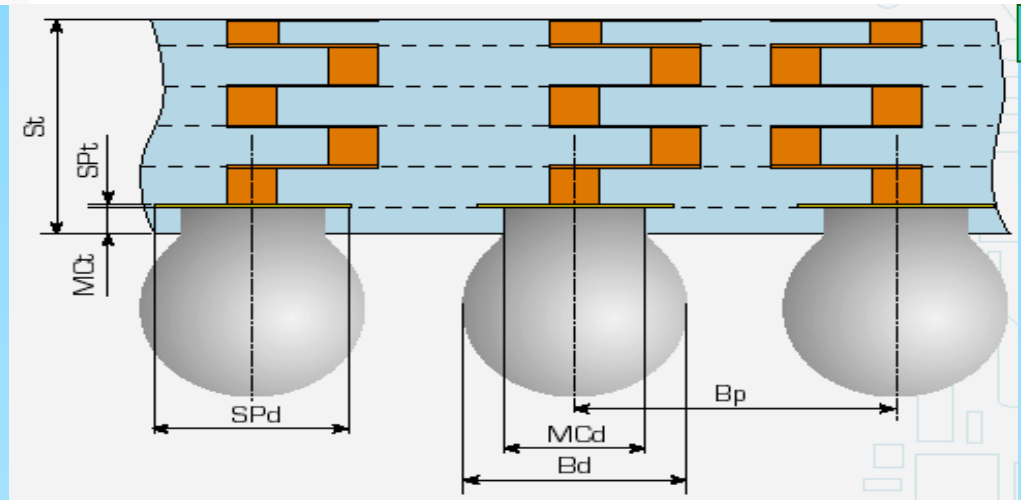


Source:Thales Microsonics

LTCC DESIGN RULES (10) BGA

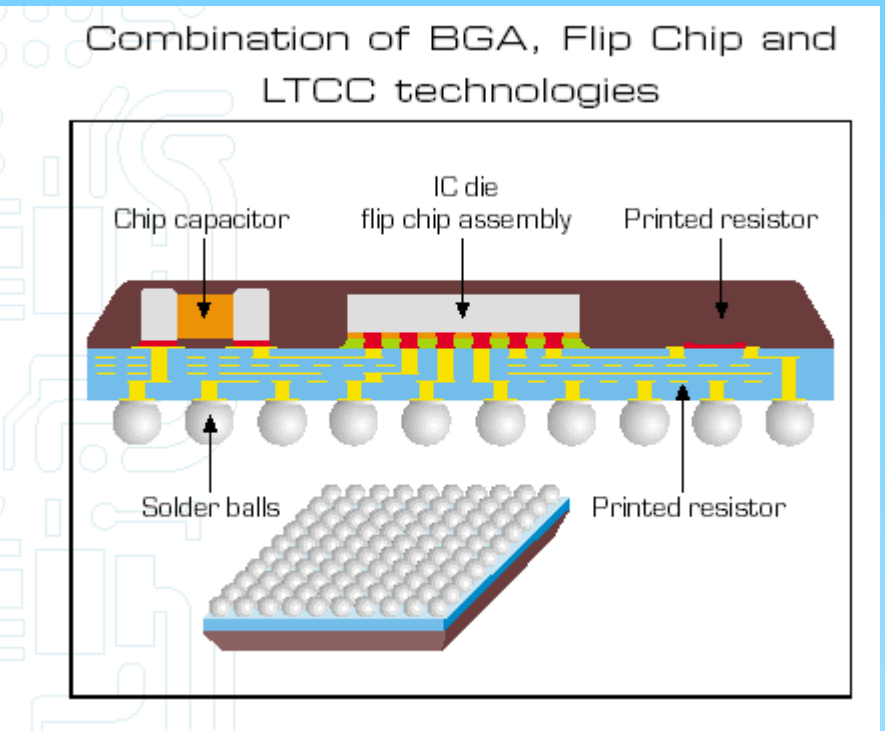


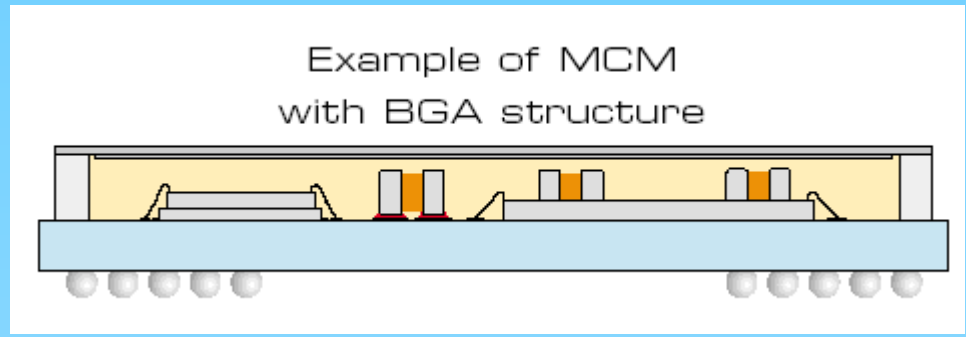
Parameter		Value	Remark
Ball pitch	Bp	1.27 mm	
Ball diameter	Bd	0.89 mm	
Micro-cavity diameter	MCd	0.57 mm	
Micro-cavity thickness	MCt	0.130 mm	
Solder pad diameter	SPd	0.770 mm	
Solder pad thickness	SPt	20 µm min.	
Solder pad material	PdAg		
Via material for layer 2	PdAg		
Conductor & via material for other inner layers	Ag		
Substrate thickness	St	0.9 mm min.	
Ball to package centre distance	BCd	20 mm max.	Depends on PCB material and temperature cycling requirements
Matrix area	MA	30 mm x 30 mm max.	For square distribution.
			Depends on PCB material and temperature cycling requirements
Substrate edge to ball distance	SEBd	0.5 mm min.	

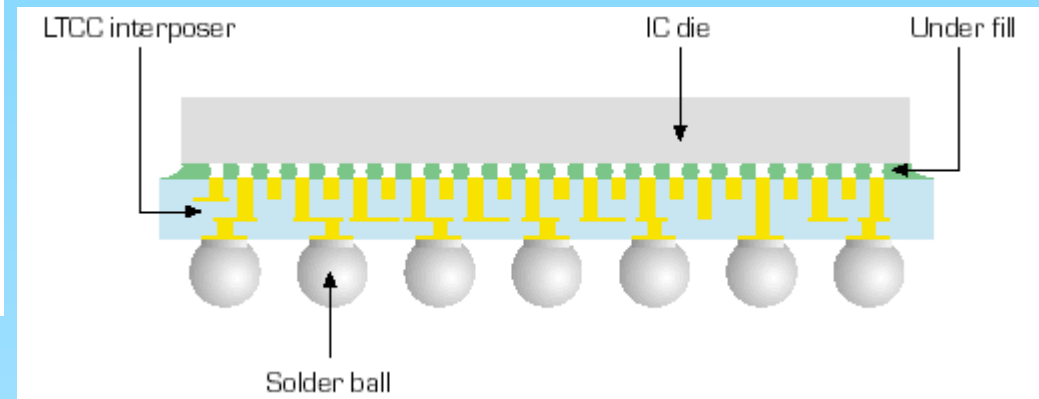


Source:Thales Microsonics

LTCC PACKAGING POSSIBILITIES







LTCC PACKAGING APPLICATIONS