

High performance current-mirror using Graded-Channel SOI nMOSFETs

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The advantages of fully-depleted (FD) SOI CMOS technology in comparison to bulk Si regarding analogue circuit design have been reported in [1]. Most of them relate to the combination of the reduced capacitance of SOI technology with the better transconductance (g_m) over drain current (I_{DS}) ratio due to the reduced FD body factor, which provides enhanced bandwidth and gain, resulting in very significantly improved micropower CMOS amplifiers. However, FD devices suffer from output impedance degradation due to the low drain breakdown [2].

One of the most important building blocks for analogue circuit operation is the current-mirror (CM), which drives current for the several circuit branches. Ideal CM operation presupposes to deliver an output current (I_{OUT}) similar to the input current (I_{IN}), independently of the output transistor drain bias (V_{DSout}), i. e. the ratio $R=I_{OUT}/I_{IN}$ closer to unity.

Due to the output impedance reduction, the performance of CM made using FD devices is significantly degraded, mainly in moderate and weak inversion regimes, which is of importance to increase the output swing in low voltage operation.

The Graded-Channel SOI MOSFET (GC) is an asymmetric channel device which has been introduced recently with the aim to reduce the inherent parasitic bipolar effects of SOI devices (Fig. 1) [3]. GC transistors indeed demonstrated significantly enhanced drain breakdown voltage, superior transconductance in saturation and significantly reduced drain output conductance [4]. In a first approximation, the device effective channel length is equal to $L-L_{LD}$ [3].

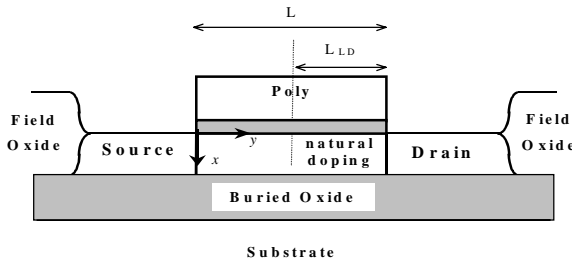


Figure 1 – Cross section of the Graded Channel SOI nMOSFET.

This work introduces the use of GC SOI MOSFET to make CM and compares its performance with CM made with conventional FD transistors.

Common-source CMs were made using both GC and FD devices, according to the 2 μ m process described in [3]. In case of GC CM, the ratio L_{LD}/L has been varied to verify such dependence on the output performance.

Fig. 2 plots the R ratio as a function of the input transistor drain voltage (V_{DSin}) for the several fabricated CM with GC and FD devices, both with $W/L=18/2$ and measured at $V_{DSout}=1.5$ V. Such curve has been obtained

by varying I_{IN} ($1nA \leq I_{IN} \leq 1mA$) and monitoring V_{DSin} , in order to cover all regions of operation. Also in this curve is included a FD CM with $L=4$ μ m.

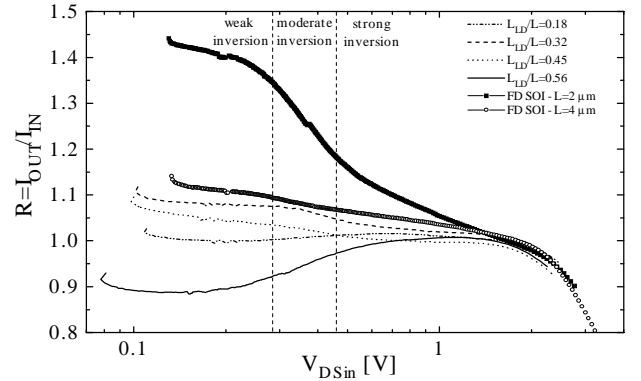


Figure 2 – Measured output to input ratio ($V_{DSout}=1.5$ V) as a function of V_{DSin} .

All the GC CM presents extremely improved output behavior in all regions of operation, even if compared to the FD CM with $L=4$ μ m.

Fig. 3 presents the I_{OUT} versus V_{DSout} curve, extracted with a constant I_{IN} of 100 μ A for the several $W/L=18/2$ GC CM with different (L_{LD}/L) and FD CM with $W/L=18/2$ and $18/4$.

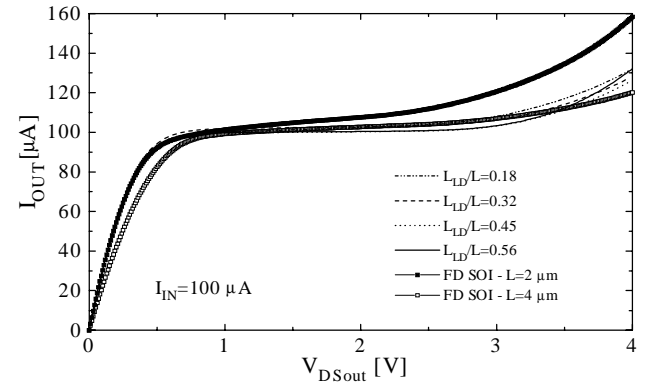


Figure 3 – Measured $I_{OUT} \times V_{DSout}$ for a constant $I_{IN}=100\mu A$.

The reduced channel length modulation and larger drain breakdown voltage of any GC transistor improves the CM output swing for similar L. For an output drain bias up to 3 V the GC CM output characteristics are closer to the FD CM with 4 μ m, which addresses the possible area reduction provided by GC transistors for similar performance.

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References

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