SIPOS passivation for semiconductor power devices

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Introduction

The major problem for the common materials used for the passivation layer in power devices is its highly insulating nature that allows the accumulation of net charge. This charge accumulation causes long-term drift of devices characteristics [1, 2].

Since its introduction in 1975 [1, 2], SIPOS process has gained a lot of interest in view of its application as a surface passivation material for high voltage and high power silicon devices. SIPOS can replace insulating dielectric passivation films, as resins, thermal silicon oxide, or glass in power devices. [2]

The conductivity of SIPOS deposited film can be slightly controlled by the quantity of oxygen incorporated into the film thus avoiding this long–term charging phenomenon [2]. The main factors, that contribute for the success of SIPOS process are: greater high voltage device stability and its compatibility with almost all-usual processes. Usually, SIPOS is deposited by low-pressure chemical vapor deposition (LPCVD) using a mixture of highly diluted SiH$_4$ in N$_2$ with N$_2$O at around 650°C.

Experimental

SIPOS films were deposited at 650°C by LPCVD using a mixture of SiH$_4$ and N$_2$O, in p-type (100), 75 mm in diameter, 1-10 Ω.cm silicon wafers. The oxygen content of the film was adjusted to be 20 at %. RBS and X-ray diffraction (XRD) analyses were performed for oxygen concentration and atomic structure measurements respectively. For MSS (Metal SIPOS Semiconductor) capacitors, aluminum was evaporated on both sides after SIPOS deposition, giving circular contacts with 1 mm$^2$ on SIPOS side of the sample and a contact covering the whole back side. For the I-V and high frequency C-V measurements, we used a HP4280 and a HP4140 system respectively.

Results and discussion

The O/Si ratio of 20 at. %, in the SIPOS films, was calculated from the measured RBS spectra. The calculated oxygen concentration in the film is similar to the one reported by Matsushita et al. [2]

In the XRD spectrum we can observe the two (100) peak from the silicon substrate and an amorphous region around 2θ=35° that is in accordance to the reference 3.

From the C-V curves, we calculated the mean effective fixed charge of the SIPOS layers as 2x10$^{11}$ cm$^{-2}$. It was possible, because the accumulation region is clearly identified.

These positive charges are induced in the SIPOS films by the p type silicon substrate and by the interface traps near the conduction band. [4]

The I-V curves confirm the semi insulating SIPOS characteristic [1], as we can observe in figure 1. The high minority carrier leakages current are in accordance to the C-V curve measurements.

![Figure 1: Typical I-V MSS capacitor characteristic](image)

Conclusion

We demonstrated that the SIPOS thin film could be obtained in an LPCVD reactor using pure silane with electrical characteristics suitable to power semiconductor device application. The mean effective fixed charge of the SIPOS layers was calculated as 2x10$^{11}$ cm$^{-2}$ and the behavior of the depletion zone demonstrates that the SIPOS layer reduces the surface electrical field.

Others experiments should be carried out to have a complete characterization of the SIPOS deposited films.

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References