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High-density plasma chemical vapor deposition of silicon-based dielectric films for integrated circuits

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In this paper, we present and review recent developments in the high-density plasma chemical vapor deposition (HDP CVD) of silicon-based dielectric films, and of films of recent interest in the development of lower-dielectric-constant alternatives. Aspects relevant to the HDP CVD process and using the process to achieve interlevel insulation, gap filling, and planarization are discussed. Results obtained thus far suggest that the process may play an important role in the future fabrication of integrated circuits, provided several metal-contamination and process-integration concerns can be effectively addressed.

Introduction

The chemical vapor deposition (CVD) of undoped and doped silicon-based dielectric layers plays a key role in the microelectronics technology. To advance the dielectric-layer-related aspects of the technology, facilitating its evolution beyond its current level of integration, advanced, low-temperature CVD processes will be needed. The processes should produce dielectric layers with minimal substrate heating (preferably lowering the "thermal budget"), have no deleterious effects on underlying gate oxides and other device structures, be suitable for filling sub-half-micron high-aspect-ratio device and circuit structures, and have reflow characteristics that facilitate the use of the chemical-mechanical polishing (CMP) used to achieve planarization. Additionally, they should require fewer process steps, thereby reducing overall fabrication costs [1].

At present, Al(Cu)-based conductor films and silicon oxide dielectric films deposited by CVD are used to produce most of the interconnections on multilevel integrated-circuit chips. To facilitate the evolution to higher levels of performance, a significant next step is underway: replacement of the Al(Cu)- based conductors with lower-resistance Cu-based conductors (see for example [2, 3]). This change reduces the RC interconnection delay significantly--by a factor of about 1.5. At present, it appears that to achieve a further significant reduction, it will be necessary to reduce the dielectric constant k of the dielectric films. It is estimated that the delay could be reduced by a factor of about 3 if the silicon oxide films, which have a dielectric constant of around 4, could be replaced by films having a dielectric constant of 2 [3]. There is, however, no clear indication of what approach should be used to achieve a reduction in k. One approach, leading to a small reduction (to a value of 3.3-3.5), involves the incorporation of a small amount of bonded fluorine in silicon oxide films deposited by HDP CVD to form a fluorinated oxide. The approach, discussed in detail in this paper, should require only a minimal change in integrated-circuit fabrication [3-7]. Other approaches, leading to a reduction of k to 2-3, involve the use of films such as carbon-doped silicon oxide [8, 9], and carbon and fluorinated carbon [10-16], deposited by either CVD or HDP CVD.

Many recent publications discuss various types of HDP sources [17, 18] and their use for dielectric film deposition and gap filling [19-34]. Electron cyclotron resonance (ECR) [19-24], helicon, helicon resonator [25, 26], and ICP sources [7, 13, 29-35] have been used for CVD process development and in early pilot line manufacturing with promising results. In submicron device fabrication, interlevel dielectric gap filling (or, simply, "gap fill") of high-aspect-ratio (>1.2)

topography generally requires the use of multistep deposition/etch or spin-on dielectric processing to produce void-free, filled structures [1]. With HDP CVD processing, high-aspect-ratio (up to 4:1) sub-half-micron structures can be filled and locally planarized in a *single* processing step. Generally, the ions and electrons from the plasma are generated at an electrode by means of an rf power source, and an rf biasing power source is applied to another (wafer-holding) electrode to create a significant ion bombardment (sputter-etching) component during deposition. For gap filling, HDP CVD processing is thus a simultaneous deposition/etching process in which loosely deposited films, or "deposited species," over planar or topographical surfaces are sputtered off by reactive ions and radicals during deposition [29, 32, 34]. The deposition/sputtering-rate ratio (*D/S*) is an important measure of the gap-filling capability of the processes. This ratio is defined as

$$D/S = (\text{net deposition rate} + \text{blanket sputtering rate})/\text{blanket sputtering rate}.$$

In general, the use of a lower *D/S* ratio facilitates the filling of a structure with a higher aspect ratio, but at a lower deposition rate.

Several commercial high-density plasma CVD systems [32, 35, 36] have been developed in connection with efforts to advance the integrated-circuit technology to the ULSI (ultralarge-scale integration) level. These systems use either ECR or ICP sources for high-density plasma generation. The advantages of each type of plasma source have recently been a subject of extensive discussions and are not covered here. Readers interested in these plasma sources, which are used in deposition and etching, may obtain more detail from recent publications [17, 18]. Since the commercial ECR system has been available for almost ten years, and deposited films and processes have been studied extensively by this author and many others [19-22, 36-38], we do not discuss additional ECR CVD results here. In this paper, the emphasis is on recent results obtained for low-temperature HDP CVD of silicon oxide and fluorinated (fluorine-doped) silicon oxide dielectric films, deposited in commercially available inductively coupled plasma (ICP) HDP CVD systems. Results for low-*k* dielectrics such as carbon and fluorocarbon deposited by HDP CVD processing are also discussed. The promising results obtained lead us to believe that HDP CVD processing may become important in the future fabrication of integrated circuits.

HDP CVD processing and equipment aspects

In our studies, HDP CVD was used to obtain films of silicon oxide and fluorinated silicon oxide. The films were formed using silane(SiH_4)/silicon tetrafluoride(SiF_4) [32]. A schematic of the reactor of the system is shown in **Figure 1**. Typical deposition conditions and properties are listed in Tables 1 and 2.

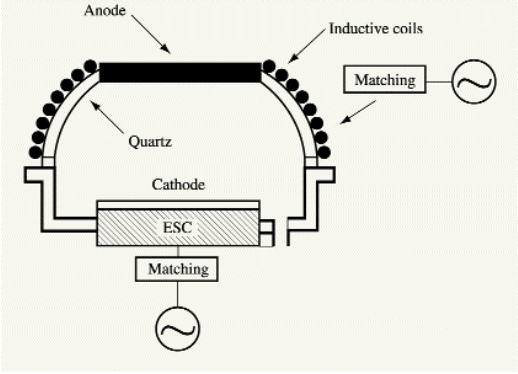

Figure 1

Schematic of inductively coupled HDP CVD reactor.

Table 1 Typical deposition conditions and properties of silicon oxide films deposited using HDP CVD.

Deposition process parameters	Value
Source rf power range	2000-4000 W
Gases	$SiH_4/Ar/O_2$ = 32-45/0-40/43-60 sccm
Pressure	<5 mTorr
Deposition/sputtered ratio	3.2:1 (filled 0.25 μm, 2.5:1 aspect ratio structure)
Deposition temperature	250-350°C
Deposition rate	180-400 nm/min
Refractive index	1.46 ± 0.003
Film stress (0.7 μm, 25°C)	(-)1.0-1.6 x 10^9 dynes/cm^2
Wet-etching rate(6:1 buffered HF)	1.6-1.8 x that of thermally grown oxide

Table 2 Typical deposition conditions and properties of fluorinated silicon oxide films deposited using HDP CVD.

Deposition process parameters	Value
Source rf power range	1000-4000 W
Gases	$SiH_4/SiF_4/Ar/O_2$=0-34/0-34/0-20/47-60 sccm
Pressure	<4 mTorr
Deposition/sputtered ratio	3.2:1 (filled 0.25 μm, >3:1 aspect ratio structure)
Deposition temperature	300-375°C
Deposition rate	130-300 nm/min
Refractive index rangs	1.43-1.47
Film stress (0.7 μm, 25°C)	(-)1.0-1.6 x 10^9 dynes/cm^2
Wet-etching rate (6:1 buffered HF)	1.5-1.9 x that of thermally grown oxide
CMP rate (oxide slurry)	1100 Å/min (1.05 x that of plasma CVD oxide)

The HDP CVD process requires the use of a relatively low pressure (2-10-mTorr range) to achieve a high electron density (10^{10} -10^{12} cm^3) and a high fractional ionization rate (10^{-4} to 10^{-1}). Because a high film-deposition rate is required for practical applications, simple initial reactant gases such as silane, silicon tetrafluoride, and oxygen are used. Complex organosilicon reactants such as tetraorthosilicate (TEOS) that are normally used in conformal plasma CVD processes [39] are dissociated into many fragmented reactive species in an HDP CVD system, increasing deposition system pressure significantly while offering little or no advantage. In order to achieve a significant deposition rate while maintaining a reasonably high sputter-etching rate for gap-filling purposes, a significant amount of initial reactant (i.e., deposited species in the plasma) must flow through the reactor, but the system must be kept at low pressure constantly during deposition. As a result, the required vacuum system must have a high pumping capability throughput and robustness: It must withstand the high temperature and high reactivity of the reaction by-products while removing them at a high rate. For an HDP CVD system, an advanced turbomolecular pump is generally required to achieve a suitable deposition rate (at low pressure) and acceptable pumping reliability [40]. The vacuum pump system is a part of the HDP CVD process that currently requires more attention.

As already noted, the HDP CVD of silicon oxide, especially under high rf biasing gap-fill conditions, produces concurrent deposition and etching. The etching and the (exothermic) silicon oxide deposition reactions each generate a large amount of heat that must be removed from the substrate during processing. For both Al-based and Cu-based sub-half-micron metal interconnects, temperature increases to above 400°C may cause significant reliability problems. For example, at temperatures above 450°C, Al-based conductors may actually start to melt. A uniform temperature across a wafer during processing is required to ensure homogenous film composition and properties over its entire area. Therefore, a major aspect of HDP CVD processing is the monitoring and

maintenance of substrate temperature. The mechanical clamp that is commonly used to retain wafers during processing would not meet the stricter requirements of heat-transfer uniformity and low particulate generation for ULSI fabrication, and would contribute to wafer bowing. Furthermore, the mechanical clamp also interferes with the plasma distribution and the gas flow, acting like a heat sink and thus possibly reducing overall process uniformity. Wafer clamping without topside contact would provide advantages regarding the reduction of particle generation and reduction of wafer-edge exclusion area (thus facilitating the fabrication of more chips on a wafer). Significant work has been done to develop various types of electrostatic wafer clamping for ULSI manufacturing [41-43]. Three configurations of interest are the unipolar, bipolar, and Johnsen-Rahbek configurations. The optimal design, configuration, fabrication materials, and process details of the configurations are closely kept secrets, with little information available [41, 42]. The HDP CVD process, with its relatively high-temperature sputter-etching and ion bombardment, requires the use of high-purity ceramic material for chuck coatings in order to effectively reduce contamination. Other high-purity ceramic, metal oxide, and other materials such as sapphire (single-crystal Al_2O_3) are also being explored for that purpose [44].

In all commercial HDP CVD equipment in current use, there is no heating element in the deposition reactor. Wafer heating is normally initiated with an Ar plasma after the wafer is loaded into the reaction chamber. After the wafer reaches the desirable temperature, which is normally in the 300-400°C range, other reactant gases are introduced to produce film deposition. Depending on the configuration of the plasma reactor and the type of wafer used, many process parameter sequences can be modified during deposition to minimize both electrical and physical damage to the topography and electronic features on the wafer [45, 46], especially on the step corner of depositing surface features. Since production is normally implemented in a batch of 25 wafers, the argon plasma is sometimes kept on constantly between runs to maintain a baseline temperature in the deposition reactor. For both silicon oxide and fluorinated silicon oxide gap-fill film-deposition processes, a gradual ramping up of rf bias minimizes physical and electrical damage. Furthermore, gradual ramping up will reduce an initial rf power surge during the initial transient phenomena of plasma-enhanced CVD processing [47, 48] that may also cause unexpected damage to devices. For deposition processes, involving volatile etching reactants such as fluorines, as in the case of fluorine-doped oxide film deposition, the etching component of the HDP CVD gap-fill process becomes significant, and the rf biasing power must be reduced, compared to the case for undoped silicon oxide, in order to prevent step corner erosion.

We have used analysis techniques such as Fourier transform infrared resonance (FTIR), Auger, secondary ion mass spectroscopy (SIMS), and nuclear reaction analysis for hydrogen [49] to analyze the film's bonding structures and composition. A Perkin-Elmer 1725X FTIR system was used to analyze the films, as described in our recent publication [50]. Auger analysis was performed on a Perkin-Elmer Model 650 scanning auger microscope with a beam voltage of 5 kV and an approximate current of 100 nA (rastered 100-µm spot size). Other film properties such as stress, wet etching, and CMP rate in conventional oxide slurry were also evaluated.

Complex multilevel 0.20-0.25-µm STI, GC, and IMD structures with high aspect ratios (1.5-3.5) were filled with HDP CVD undoped silicon oxide. In the case of IMD structures, lower dc fluorinated silicon oxide films were also used for the gap-fill deposition. These structures were subsequently processed to several metal levels and then evaluated for dielectric gap fill, CMP integration, and plasma damage on 80-100-Å gate-oxide devices. The results were compared to those for the same device structures processed with conventional LPCVD SiO_2 or plasma CVD oxide gap-fill processing.

Plasma-CVD-induced damage was also measured using the antenna structures as dielectric test site (DTS) monitors containing large-area polysilicon capacitors and antenna devices with areas ranging from 0.2 to 0.001 cm^2. The antenna ratio is defined as the ratio of the polysilicon gate area to the

thin gate-oxide area. The antenna devices on DTS monitor wafers have ratios of 0.2, 1, and 10 M (million). The higher the antenna ratio, the more sensitive the devices are to plasma damage. Details of the fabrication process and structure of these DTS monitors have recently been presented [51]. Intra and inter-level dielectric constants have also been measured using fingered comb structures with spacings ranging from 0.50 to 10 µm, as described in a previous publication [52]. The results were also confirmed with 0.25-µm Al(Cu) interconnect patterned test structures.

Deposited film characterization and properties

• *Undoped silicon oxide films*

Silicon oxide films were deposited using a silane/oxygen/argon gas mixture. Besides parameters associated with the design of the system, the inductive coil, and the plasma source, there are several principal process parameters that affect the deposited film properties: substrate temperature, reactant gas ratio, rf biasing power, and deposition pressure. FTIR analysis showed that films deposited under the conditions of Table 1, with high oxygen/silane ratios, display no water absorption and a small amount of O-H bonding (3674 cm^{-1}), as indicated in **Figure 2**. The Si-O stretching band (1085 cm^{-1}) half-peak- width maximum is typically small (88 cm^{-1}). The indicated HDP CVD film bonding features are similar to those of conventional high-temperature LPCVD SiO_2 films deposited at 650-700°C. These HDP CVD films also display uniform and stoichiometric silicon dioxide compositions and hydrogen concentrations typically ranging from 1.5 to 2.0 atomic percent (at.%) depending on deposition conditions.

Typical Auger electron spectroscopy (AES) and hydrogen depth profiles are shown in **Figures 3** and **4**, respectively. The Auger depth profile composition is highly uniform, indicating a good process control. Wet etching in buffered HF solution (6:1 of water:buffered HF) indicated less than a ±5% variation in etching rate with depth and across a 200-mm-diameter wafer. The wet-etching rate in this solution is about 1.6-1.8 times that of thermally (950°C) grown oxide films. It should be noted that conventional plasma CVD films have a wet-etching-rate ratio of 1.7 to 2.0 compared to that of thermally grown oxide. These results confirm that films of improved quality and consistency can be deposited by HDP CVD.

Films deposited with a higher rf bias power and temperature range (Table 1) display a denser bonding structure and lower hydrogen content. The denser bonding structure is indicated by a more gradual Auger depth profile, slightly less Si-O HPWM bonding, and a lower buffered HF wet-etching rate at similar stoichiometric SiO_x compositions. Films deposited with a high oxygen/silane flow ratio (oxygen-rich region) display a refractive index near 1.46 and uniform silicon and oxygen stoichiometric SiO_2 profiles.

During the first few silicon oxide deposition runs on blanket silicon wafers, SIMS analysis showed no significant metal contamination ($<1 \times 10^{15}$ cm^{-3}) in deposited films. However, after the equipment was used to deposit films on ILD wafers with Al(Cu)-based metallization patterns, SIMS analysis indicated some aluminum contamination in the 1×10^{16}-cm^{-3} range and some Cr at Si interfaces but with no significant carbon, iron, copper, or nickel contamination (**Figure 5**). Therefore, the Al contamination may have arisen from the Al(Cu)-based metallization on patterned wafers that was sputtered off during the initial Ar plasma heating period of the HDP CVD processing sequence, as discussed previously. Even for an HDP CVD system that had not been exposed to patterned, metallized wafers, a slight increase in aluminum and other metal contamination in the deposited films has been observed after prolonged operating periods. Such contamination has been traced to several equipment parts such as the inductive plasma dome and the electrostatic chuck. During the heating and deposition process, materials such as the alumina overcoat may be sputtering off the parts via high-energy ion sputtering, especially when high-aspect-ratio gap fill is required. Such low-level metal contamination is not an issue for ILD applications. However, it is of considerable concern in connection with ULSI device and circuit

requirements, with regard to both STI and GC gap-fill applications. Even at low levels (contamination in the 1 x 10^{16}-cm^{-3} range), it will degrade device performance and reliability. This metal contamination can be reduced by depositing a thin silicon oxide passivation film after the plasma-cleaning step. For ICP HDP CVD systems containing an alumina or silica dome within which rf power is applied, the metal contamination in the material that is used to fabricate the dome may leach out into the deposition system after many hours of operation. Therefore, if the process is to be used for STI and GC gap fill, it will be necessary to carefully monitor the level of metal contamination and devise means to reduce it to an acceptably low level (<1 x 10^{15} cm^{-3}) in the deposited films.

For HDP CVD silicon oxide films deposited with high *D/S* and oxygen/silane ratios (and with a refractive index in the 1.462 ± 0.002 range) that fill 0.25-2.0-µm structures with a 2:1 aspect ratio, inter- and intra-level dielectric constants are found to be 4.00 ± 0.05 using fingered comb structures with spacings ranging from 0.50 to 10 µm [52].

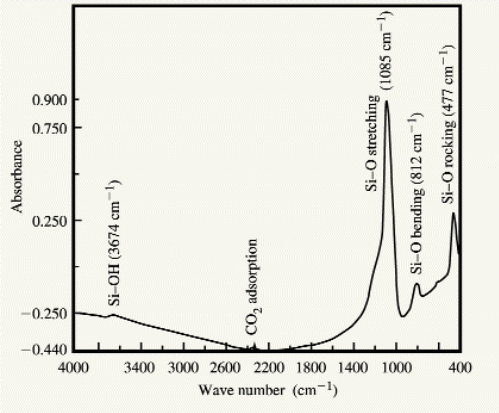

Figure 2

FTIR spectra of a typical silicon oxide film deposited using HDP CVD.

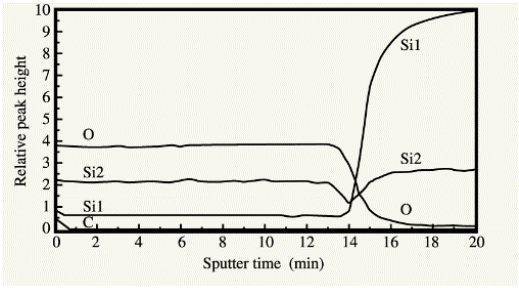

Figure 3

AES depth profile of a typical HDP CVD silicon oxide film. The designations Si1 and Si2 pertain to different Si peaks. The carbon peak is essentially at the noise level.

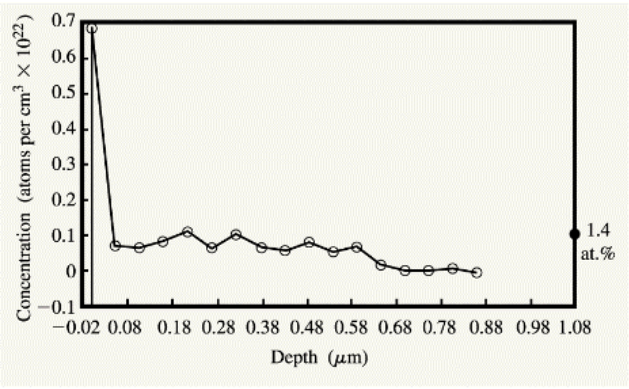

Figure 4

Hydrogen depth profile of a typical HDP CVD silicon oxide film.

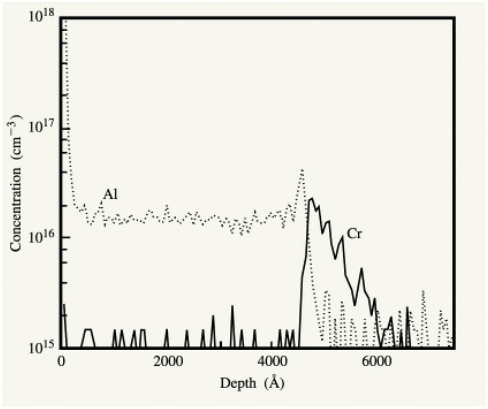

Figure 5

SIMS analysis of a typical 5000-Å-thick HDP CVD silicon film before and after CMP. No Cu, Ni, or Fe was detected.

Chemical-mechanical polishing (CMP) results have indicated that the CMP rate for HDP CVD oxide in a conventional oxide slurry is about 1100 Å per minute, comparable to those for plasma CVD silane-based oxide films. A typical thickness measurement of a blanket HDP CVD oxide film before and after removal of about 1300 Å of oxide by CMP showed no significant degradation in film uniformity (**Figure 6**).

In order to study plasma-induced damage to device structures, multilevel 0.25-µm STI, GC, and IMD structures filled with HDP CVD silicon oxide films were examined. Results obtained were similar to those obtained when use was made of conventional thermal LPCVD processes. The breakdown yield was above 90% even after a 10-MV/cm field was applied to the gate-oxide films. Electrical yields of polysilicon 100-Å-thick gate-oxide capacitors with 0.2, 2, and 10M:1 antenna ratios were also high (>90%). A schematic of the test structure used is shown in **Figure 7**, and the results obtained are summarized in Table 3. The HDP CVD conditions used were those listed in Table 1. The results obtained indicated that the HDP CVD processing did not cause any significant damage to 80-100-Å- thick gate oxides under various processing conditions suitable for filling high-aspect-ratio 0.25-µm Al(Cu)-based interconnect gaps. More recent data have shown that no significant plasma damage is observed to 50-Å-thick gate oxides under similar process conditions. Overall, the gate damage caused by HDP CVD processing has been found to be much smaller than that from conventional plasma CVD processing at a lower rf power density.

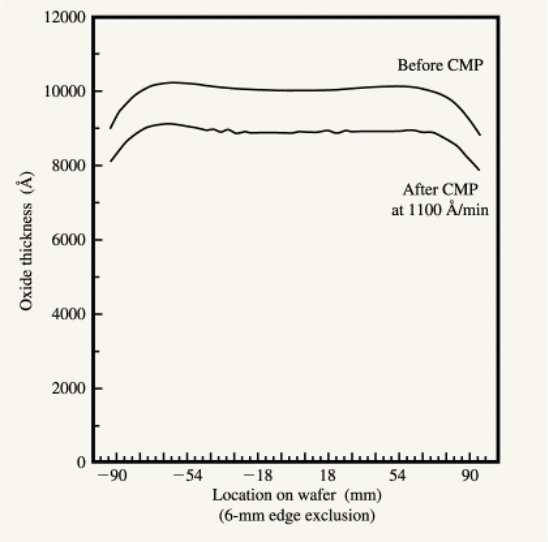

Figure 6

Thickness profile (across a wafer) of a typical HDP CVD silicon oxide film, before and after CMP.

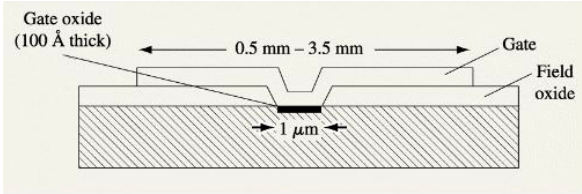

Figure 7

Schematic of test structure used for plasma damage investigations.

Table 3 Electrical yields of polysilicon 100-Å-thick gate-oxide capacitors having antenna ratios of 0.2M:1, 2.0M:1, and 10M:1.

Run number	Conditions	Yield (%)			Comments
		0.2M:1	2.0M:1	10M:1	
1	A	100	98	100	Good
2	B	100	100	95	Good
3	C	100	100	100	Best result
4	D	100	98	98	Good
5	E	100	100	90	OK (lowest)
6	F	100	100	95	OK
Control	No plasma process	100	100	100	OK

• *Fluorine-doped silicon oxide films*

Generally, HDP CVD fluorinated silicon oxide (hereafter referred to as "fluorinated oxide" or "F-oxide") films can be deposited by gas precursors containing SiF_4/O_2 or an $SiF_4/SiH_4/O_2$ combination. Our recent work [6, 7, 53, 54] and that of others [55-57] has shown that the presence of hydrogenated reactants in the gas precursors improves that stability of fluorinated oxide films. The hydrogen in the discharge appears to remove the excess fluorine and enhance the film stability. Without the hydrogen from an initial precursor suchas H_2 or SiH_4, the fluorinated oxide films generally display a slightly lower deposition rate and absorb water more readily than under conventional plasma CVD conditions. By using a $SiF_4/SiH_4/O_2$ precursor, relatively high fluorine concentrations (up to 14-15 at.%) can be incorporated into the silicon oxide bonding network while still maintaining film stability. This stable fluorine incorporation is due to the direct insertion of Si-F bonding units, forming from SiF_4 dissociation, into the Si-O bonding network. Excess fluorine from SiF_4 dissociation is also effectively removed by excess hydrogen from SiH_4 dissociation. During HDP CVD processing, as already indicated, deposition and etching occur simultaneously at the substrate surface. The deposition species are formed from reactions between reactive species of SiH_4(2% in argon)/SiF_4/O_2 generated in the plasma. Fluorine etching species are produced from SiF_4 dissociation. Although the etching yield of deposited oxide films is much smaller than when C_2F_6 is used [6], the etching component is still quite high under high rf and rf-biasing power levels and/or large SiF_4 flow. Under such conditions, increased ion bombardment and fluorine dissociation enhance the etching component, thus effectively reducing the deposition rate and the amount of fluorine incorporated in the films.

Parametric studies of the deposition rate, refractive index, fluorine incorporation, and Si-F and Si-O bonding variations with deposition parameters [rf power (forward and bias), gas-flow ratios, substrate temperature, etc.] show that the amount of fluorine incorporation in the film is strongly influenced by the SiF_4/SiH_4 ratio and the rf power used. The substrate heating by the initial Ar plasma has a significant effect on the amount of fluorine incorporated and its stability in the films. F-oxide films deposited at a higher processing temperature (Table 2 conditions) contain less fluorine. Under the same process conditions, the fluorine incorporation in the films increases with increasing SiF_4 flow and decreases with increasing rf bias power and inductive power. **Figure 8** shows a typical effect of rf biasing power on the deposition rate at three SiF_4 flow ratios under the conditions of Table 2. It can be seen from the results that ion bombardment (i.e., sputtering effect) has a significant effect on the deposition rate. As in a conventional plasma CVD process, HDP CVD fluorinated oxide deposition process parameters can be changed to optimize film properties for specific applications. **Figure 9** shows typical FTIR spectra of F-oxide films deposited at 1 and 2.5 kW of rf biasing. These spectra indicate film stability and show the presence of Si-F (945 cm^{-1}), Si-OH (silanol, 3670 cm^{-1}), and Si-O (460, 835, and 1130 cm^{-1}) bonds with no water absorption. **Figure 10** shows the effect of rf biasing power on the amount of silanol bonding in five films. The decrease with rf power may have been due to increased ion bombardment during film deposition. An increase in SiF_4 flow ratio from 15 to 29% also decreased the silanol concentration. In both cases, the hydrogen was removed either by ion bombardment or by the presence of fluorine species generated during SiF_4 dissociation. It should be noted that stable F-oxide films deposited with SiF_4/O_2 initially contained no silanol but slowly absorbed water (hydrolyzed) upon exposure to high humidity. The absorption was less if the films were capped by undoped oxide or the concentration of fluorine on exposed surfaces was lower. Under our baseline conditions, HDP CVD F-oxide films deposited with a greater SiF_4 flow level or more rf power displayed less silanol bonding and did not absorb water upon exposure to air ambient. **Figure 11** shows typical AES depth profiles of HDP CVD F-oxide films deposited at SiF_4 flow levels of 29% and 100%. It can be seen that the fluorine concentration was lower at the film interface and surface, thus enhancing film stability. Analysis indicated a slightly lower hydrogen content in F-oxide films (0.5-1.4 at.% vs. 1-1.6 at.% for silicon oxide films), as shown in **Figure 12**. With regard to metal contamination, similar results were observed in both silicon oxide and fluorinated oxide films, as discussed previously. The wet-etching

rate in buffered HF and the chemical-mechanical polishing rate in an oxide slurry are indicated in Table 2. In our CMP study using blanket HDP CVD F-oxide films deposited with a SiF_4 precursor and with a 5-6 at.% fluorine concentration, no significant interaction between the slurry and the films was observed, and the CMP rate was increased only slightly. However, it should be noted that a recent report [58] has indicated that plasma CVD F-oxide films deposited with a C_2F_6 precursor and with 8-9 at.% fluorine concentration show more sensitivity to CMP. CMP rates up to 30% higher were observed for F-oxide films compared to undoped films, and the rate increased with increasing fluorine concentration. The increased CMP rate was attributed to the increased hydrolysis of Si-F bonds in the CMP slurry solution.

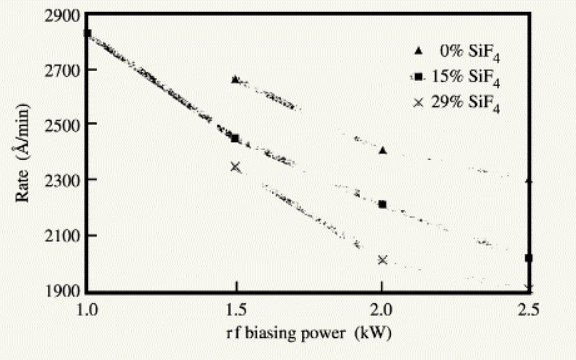

Figure 8

Typical effects of rf biasing power on the deposition rate of HDP CVD fluorinated silicon oxide films.

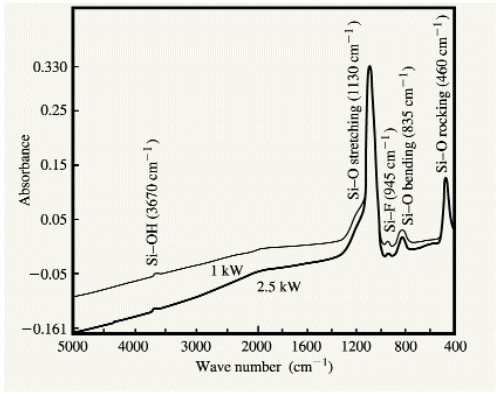

Figure 9

FTIR spectra of typical HDP CVD fluorinated silicon oxide films deposited at two rf biasing power levels.

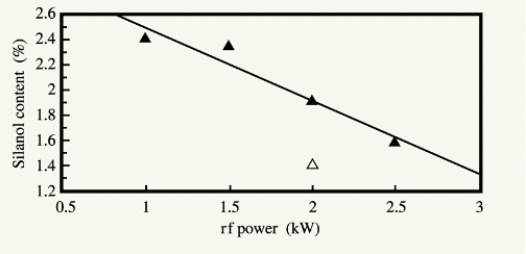

Figure 10

Illustrative effect of rf biasing power on silanol content of typical HDP CVD fluorinated silicon oxide films. Fluorine levels in the films were 15% (solid triangles) and 29% (open triangles).

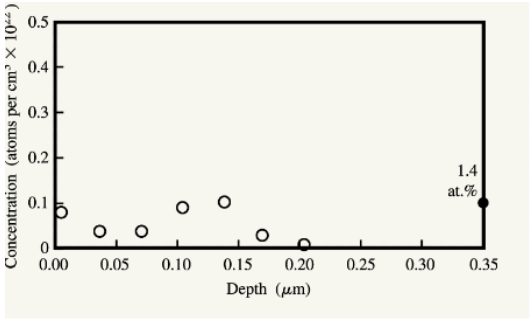

Figure 12

Hydrogen depth profile of a typical HDP CVD fluorinated silicon oxide film.

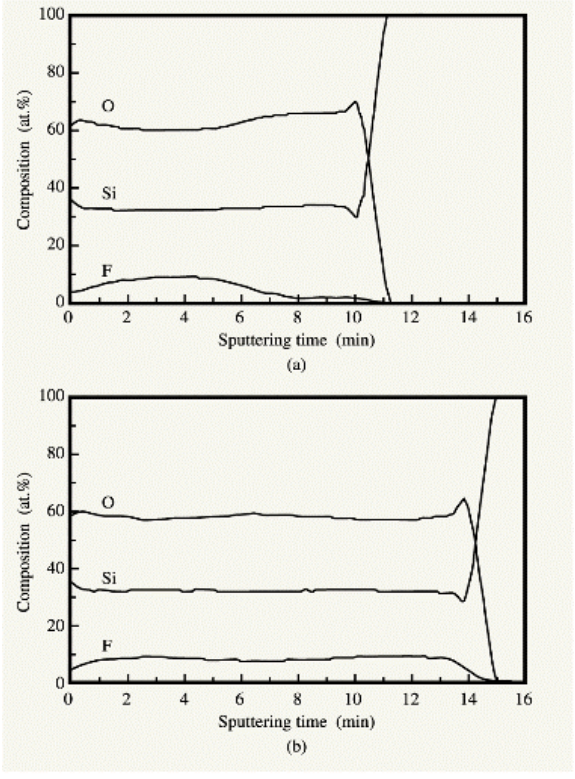

Figure 11

AES depth profiles of typical HDP CVD fluorinated silicon oxide films deposited at SiF_4 flow levels of (a) 29% and (b) 100%.

In a recent study, we have found that F-oxide films deposited by conventional plasma CVD with similar precursors but without a hydrogen source [i.e., SiF_4/O_2 (or N_2O) only] display relatively low deposition rates and absorb water more readily upon exposure to air [54]. With conventional plasma CVD processing, a hydrogen source is needed to increase both film stability and deposition rate. However, in HDP CVD, where increased electron dissociation of SiF_4/O_2 precursors and increased ion bombardment of deposited films on the substrate occur, slightly less stable F-oxide films can be deposited with or without the addition of a hydrogen (H_2 or SiH_4) precursor, but at a lower deposition rate and with less fluorine incorporation in the films. For HDP CVD fluorinated silicon oxide film deposition, increased ion bombardment during deposition (by increasing rf bias power) increases film stability but reduces the amount of incorporated fluorine and the deposition rate. The concentration of incorporated fluorine, its bonding structure, and its depth profile in the deposited film have significant effects on film stability. The fluorine depth profile, concentration, and bonding can be manipulated to improve stability with suitable deposition conditions. Another study [59] has indicated that a suitable amount of fluorine incorporation was shown to passivate and neutralize any trapped charge existing in HDP CVD oxide films, thus increasing the film breakdown voltage. However, too much fluorine incorporation in the films results in the formation of a porous oxide network and hole traps, and eventually causes device reliability problems. It is possible to modify process conditions to enhance F-oxide film stability. For example, surface treatment of fluorinated oxide films by nitrous oxide plasma exposure reduces the fluorine concentration on the film surface and improves adhesion by subsequently deposited films [60].

Overall, our HDP CVD oxide films deposited with $SiF_4/SiH_4/O_2$ precursor chemistry appeared to be more stable than films deposited with other fluorine precursors such as CF_4 or C_2F_6. The enhanced stability of our fluorine-doped oxide films can also be attributed to the use of Si-F bonding precursors [6, 53]. Precursors with Si-F bonding, such as SiF_4, dissociate to form Si-F precursors in an HDP discharge. Subsequently, the Si-F species will incorporate directly at the Si-F bonding unit in the film surface without going through fluorine reactive species formation and incorporation in the F-oxide film, as in the case of a CF_4 precursor. Since the Si-F species is generated and then subsequently bonded (incorporated) directly into the film, the overall Si-F bonding energy change is lower. This is probably responsible for the enhanced film stability observed in F-oxide films deposited with an Si-F precursor under various deposition conditions.

In general, the chemical aspects of plasma deposition are complex and involve many reaction steps [61], especially in HDP CVD. Furthermore, active fluorine etchant species (F, SiF_x, HF, etc.) act as etching or deposition species both in the discharge chamber and on the substrate surface under a suitable selection of process parameters. However, our results and those of others [7, 54-57] suggest two principal mechanisms that may be used as a general guideline to obtain more stable fluorinated oxide films: a) the insertion of more stable and direct Si-F bonding species into the films (this can be accomplished by suitable deposition precursors with Si-F bonding [6, 7, 53]); and b) facilitating the removal of excess fluorine generated in the plasma discharge by including hydrogen-based precursors (hydrogen, silane, etc.) to form more volatile species such as H-F, and enhanced ion bombardment (by increasing HDP rf biasing power) to remove or/and to densify loosely bonded F species in the film.

Stable fluorinated silicon oxide films with up to 10 at.% fluorine can be deposited for high-aspect-ratio >= 3:1) gap fill using this approach. Up to 15 at.% fluorine can also be incorporated into the oxide film using HDP processing, but these films tend to be less stable (i.e., absorb moisture upon long-term exposure in air) than films with 5-10 at.% fluorine. The measured dielectric constants of the latter films are in the 3.4-3.6 range [52]. Another study [62] has predicted that the dielectric constant of F-oxide films should be reducible to a level as low as 2.6; the prediction was based on a Kramer-Kronig calculation. However, experimental electrical *C-V* measurements on F-oxide films

have failed to produce so low a value. Reported *k* values range from 3.1 to 3.7, depending on process conditions. These values are more consistent with the *ab initio* calculation by Lucovsky and Yang [63], which showed that 10-12 at.% incorporation of fluorine in silicon oxide films should reduce the *k* value to the 3.2-3.4 range. It should be noted that both calculations do not include the effect of -OH incorporation in the F-oxide films; that should increase the dielectric constant. For less stable F-oxide films, the slow absorption of water vapor in air increases *k* with time. It should be noted that in the recent report mentioned above [64], fluorinated silicon oxide was used as a low-*k* dielectric material for fabricating multilevel logic devices.

• *General properties of carbon- and fluorine-doped carbon films**

As mentioned previously, the development of low-*k* dielectric materials is of current interest in attempting to improve the performance of integrated circuits. Both conventional plasma CVD and HDP CVD carbon and F-doped carbon (F-C_x) films have been identified as excellent candidates for low-*k* dielectric materials for multilayer interconnections at ULSI levels of integration [16, 65-67]. The deposition temperatures of these films are normally below 420°C to minimize deleterious effects on metallic and insulating layers that may be present on the substrate. The dielectric constants of those carbon and fluorocarbon films are reported in the range of 2.0 to 3.3, with carbon films in the upper range and fluorocarbon films in the lower range. The carbon and fluorocarbon films are generally deposited with individual precursors or a combination of various types of hydrocarbon and fluorocarbon precursors such as methane (CH_4), ethylene (C_2H_4), CF_4, C_2F_6, $C4F_8$, CHF_3 with Ar and hydrogen [10, 12, 13, 15, 16, 65-68]. Other ring-type hydrocarbon fluorocarbon compounds such as benzene (C_6H6), difluorobenzene ($C_6F_4H_2$), and hexafluorobenzene (C_6F_6) [11, 69], and even oxygenated fluorocarbon such as hexafluoropropylene oxide (HFPO, C_3F_6O) [14] have also been used as precursors. Thus far, no significant advantages in carbon and fluorocarbon film properties have been observed for films deposited by conventional plasma CVD compared to films deposited by the high-density plasma process. The only advantage of the high-density plasma process noted thus far has been improved gap fill [13, 16]. Since low-*k* dielectric properties of carbon and fluorocarbon film are controlled by the film bonding structures and the F/C ratio, it is actually more difficult to control the film properties and deposition rate using HDP CVD processing because of significantly high dissociation rates and concurrent ion bombardment.

For low-*k* dielectric carbon films, controlling the ion bombardment and film bonding structures drastically affects the *k* value [11, 13, 67]. It should be noted that the rf power and processing temperature are generally much lower than in the HDP CVD process used in diamondlike carbon deposition [70].

Carbon film thermal stability, stress, and dielectric constant are strongly related to deposition conditions (precursors, rf bias, power density, etc.), bonding (sp_3 vs. sp_2 bonding), density, and composition (H/C ratio). Films with more sp_2 bonding and a higher H/C ratio tend to have a lower *k* value and less thermal stability [11, 67] compared to those with more sp_3 bonding. The optimization of film adhesion, thermal and chemical stability, film stress, and *k* value has been investigated [11, 13, 16]. The incorporation of small amounts of silicon into a carbon film will enhance its stability and adhesion [11, 16]. However, the incorporation of silicon increases the film's dielectric constant. In a study in which both carbon- and silicon-doped carbon films were used as adhesion layers for low-*k* fluorocarbon dielectrics [11, 13, 16], the carbon films were found to be more stable thermally and chemically than fluorocarbon films, but their dielectric constants were found to be higher.

For fluorocarbon films, the plasma-deposition process and precursor chemistry play a significant role in film stability. In general, films deposited with a high F/C ratio tend to have a lower dielectric constant but poorer thermal stability and adhesion. So far, the fluorocarbon films tested for integrated-circuit use have required underlying, adhesion-promoting layers. Suitable precursor gases such as (C_2H_2) + $C4F_8$ [68], difluorobenzene ($C_6F_4H_2$), and hexafluorobenzene (C_6F_6) +

Ar/H_2 [11] produce films with a low dielectric constant but with higher stability compared to films deposited with CHF_3 and/or fluorocarbon gases such as CF_4, C_2F_6, or $C4F_8$ [10, 70]. The addition of hydrogen or hydrocarbon precursors in addition to fluorocarbon precursors helps remove excess fluorine generated in the plasma dissociation of fluorocarbon and enhances the cross-linking bonding density in the films [65]. This subsequently increases the glass transition temperature (T_g) and film thermal stability. Recently studies [14, 71] have shown that pulse-plasma-enhanced CVD can be used to deposit fluorocarbon films using a hexafluoropropylene oxide (HFPO = C_3F_6O) precursor. With varying plasma-pulsing excitation times, fluorocarbon films with a low dielectric constant, low dangling-bond concentration, and highly stable -CF_2 bonding in the film bulk can be deposited in a controllable process. More stable fluorocarbon films with *k* values as low as 1.95-2.0 can be deposited using the process. Current ULSI test devices using HDP CVD fluorocarbon dielectrics required several adhesion layers (a-Si, a-C) and low-*k* fluorinated oxide dielectrics to achieve completed multilevel integrated metallization structures [16]. Recent results [13] have shown that HDP CVD processing can be used to control and to alter the chemical, optical, and mechanical properties of both carbon and fluorocarbon films. Owing to the chemical bonding structure of the fluorocarbon film system, it is unlikely that most fluorocarbon films will be stable above 420°C. Therefore, for ULSI fabrication, subsequent deposition and annealing processes after low-*k* fluorocarbon film deposition would have to be carried out below this temperature. If CVD carbon and fluorocarbon films are to be selected for use in integrated-circuit processing, it is likely that these films will have to be integrated with copper-based interconnections at submicron dimensions using damascene processing [72, 73]. If that is the case, for CVD carbon and fluorocarbon films, HDP CVD processing would provide little advantage compared to conventional plasma CVD processing. Whatever the case, hydrogenated carbon and fluorocarbon films deposited by HDP, conventional plasma, or thermal CVD processes [74] currently appear to be attractive candidates for the low-*k* dielectrics that will be needed to advance the integrated-circuit technology.

HDP CVD dielectric gap-fill applications

In recent years, the achievement of void-free gap fill has been critical in the advancement of the integrated-circuit technology. Current developments in HDP CVD, ozone/TEOS CVD, and advanced spin-on glass are focusing on void-free gap fill of high-aspect-ratio (>2:1) sub-half-micron structures. For HDP CVD dielectric gap fill, development work is focused on interlevel insulation [4, 30, 75], gate conductors [76, 77], and shallow-trench isolation structures [45, 78].

• *Interlevel dielectrics*

As already noted, HDP CVD is a simultaneous deposition/etching process. The deposition/sputter-rate ratio (*D/S*) is an important parameter with respect to the gap-filling capability of the processes. For 0.25/0.18-µm structures with 2-2.5 aspect ratios, the best gap filling is achieved with a *D/S* ratio in the 3.0-3.5 range. **Figures 13** and **14** show typical 0.25- and sub-0.25-µm Al(Cu) interconnection void-free gap-fill structures. It can be seen that the gap-fill process is highly directional, with a "bottom-up" fill profile, as has also been observed by others [21, 37]. In a dense metal pattern, partial local planarization can be obtained over the structure using a high *D/S* level (Figure 13). However, truly global planarization of sub-half-micron structures requires an additional CMP step. In IBM, high-density-plasma CVD interlevel dielectric (ILD) oxide layers have been introduced into 0.35-µm logic and SRAM manufacturing [79] with excellent gap-fill capabilities. For integrated 0.25- and sub-0.25-µm interconnections, HDP CVD processing showed superior gap-fill capabilities compared to sub-atmospheric $TEOS/O_3$ processing [33, 80] and required fewer processing steps than a spin-on-polymer etch-back process [81]. No significant increase in gate breakdown failure rate was observed for 0.25- and 0.35-µm devices having a 50-65-Å-thick gate oxide and coated with an HDP CVD oxide ILD [29, 33, 81]. For F-oxide films, high- aspect-ratio (>2.5:1) 0.20-µm void-free gap-fill Al(Cu)-based interconnection structures can easily be achieved (**Figure 15**). Thin (100-300-Å-thick) plasma-deposited oxide films are used prior to F-oxide film

deposition to enhance adhesion and prevent interaction between the F-oxide, the Al(Cu), and the thin metallic liners that are used. A recent study [82] has shown that integrated HDP CVD F-oxide and CMP can be used to fabricate a planarized 0.25-µm Al(Cu)-based metallization structure including a 150-nm capping silicon oxide layer. The capping oxide layer is needed to enhance the adhesion to an overlying interconnection layer. The seed and capping layers also prevent any reactive fluorine which may be present at the upper and lower interfaces of the F-oxide from causing degradation during subsequent annealing steps. The measured dielectric constant of HDP CVD F-oxide films we have deposited over 0.25-µm Al(Cu) lines is about 3.55-3.6. A slightly lower value, 3.46, has also been reported [82].

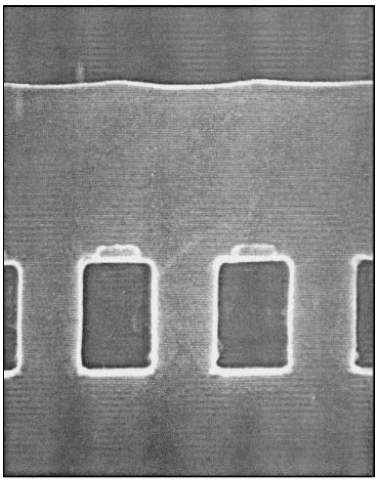

Figure 13

SEM cross-section micrograph illustrating gap filling and local planarization that can be achieved by HDP CVD of silicon oxide over 0.25-μm-wide Al(Cu)-based lines.

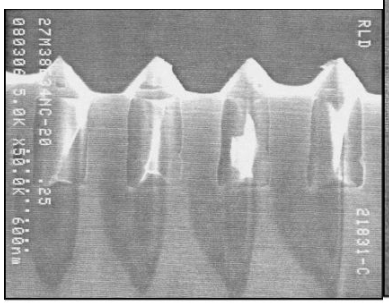

Figure 14

SEM cross-section micrograph illustrating gap filling that can be achieved by HDP CVD of silicon oxide over sub-0.25-μm-wide Al(Cu)-based lines.

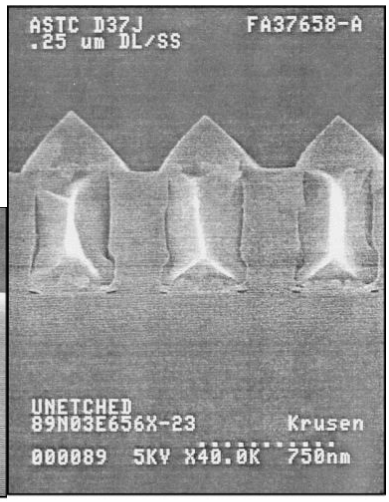

Figure 15

SEM cross-section micrograph illustrating gap filling that can be achieved by HDP CVD of fluorinated silicon oxide over 0.25-μm-wide Al(Cu)-based lines.

• *Gap fill for gate conductors (pre-metal dielectrics)*

For gate conductors, both undoped and doped (with phosphorus and/or boron) silicon oxide have been used for gap fill [1]. In our evaluation, HDP CVD undoped silicon oxide was used to study the gate-conductor (GC) gap fill [29]. If the *D/S* ratio is high, some corner erosion of the gate-conductor structure occurs: The corners become rounded as a result of Ar^+ bombardment during the initial few seconds of the HDP CVD [47, 48]. The rounding can be avoided by CVD of a thin conventional plasma silicon oxide layer prior to HDP CVD. After the gap structures are filled by HDP CVD of silicon oxide, conventional plasma CVD silicon oxide films are used to partially smooth the surface for subsequent CMP. **Figure 16** shows a completed GC structure fabricated using such an initial oxide and subsequently planarized by CMP. Note that it is also possible to ramp up the rf biasing slowly for the first 5-10 seconds of the deposition process to minimize the Ar^+ bombardment and thereby avoid the GC corner erosion. In recent studies, both HDP CVD undoped and phosphorus-doped silicon oxide (PSG) dielectrics deposited at 350-

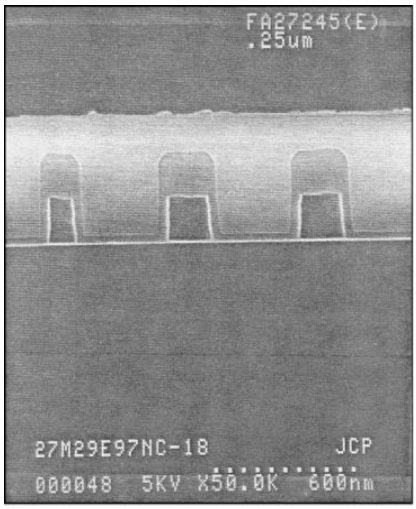

Figure 16

SEM cross-section micrograph illustrating gate-conductor gap filling and coating achieved after the following steps: deposition of a relatively thin silicon oxide layer by conventional CVD to protect metal line corners; deposition of a second silicon oxide layer by HDP CVD for gap filling; deposition of a third silicon oxide layer by conventional CVD for partial smoothing; and CMP for planarization.

400°C have also been used as gap-fill materials for ULSI devices [76, 77]. In one study, a composite HDP CVD silicon undoped oxide gap fill and plasma-CVD-doped silicate glass film were deposited and successfully integrated into a 0.25-µm CMOS device process to achieve better pre-metal GC gap fill while causing no degradation impact on the CMOS device performance [76]. For HDP CVD PSG films with phosphorus concentrations in the 3.5-6.5 wt.% range, subsequent annealing at higher temperature (700°C) was required for film stabilization. An extensive gap-fill and film characterization study of HDP CVD PSG on CMOS devices indicated improved gap fill at lower processing temperatures compared to CMOS devices processed with higher-temperature (850°) CVD BPSG films [77]. Because of the excellent gap-filling capability of the HDP CVD PSG process and its low thermal budget, it offers another promising alternative to current TEOS/O_3 BPSG or conventional CVD BPSG as a pre-metal dielectric CVD process for sub-0.25-µm circuits, provided metal contamination can be kept to a minimal level.

• *Gap fill for shallow-trench isolation*

Until recently, the low-pressure CVD TEOS/O_2 process had been used to deposit high-quality silicon oxide dielectrics for shallow-trench isolation (STI) in ULSI devices [83]. As the aspect ratio for the STI structures becomes larger (>1.2:1), the standard LPCVD process no longer meets gap-fill requirements. With an advanced TEOS/O_3 CVD oxide gap-fill process, higher- aspect-ratio sub-half-micron structures with a gradual sloped profile can be filled without voids [1]. For STI, the consistency of void-free gap fill has a very significant effect on the subsequent STI integration process steps and on final device yield and performance. To improve ULSI CMOS device performance and packing density, vertical STI slope structures with a higher aspect ratio (2:1) must be filled with void-free high-quality oxide dielectric. In this case, the advanced TEOS/O_3 CVD process may not satisfy that requirement, causing the STI gap-fill structures to form a void in a fill center [45]. This void at the center of the filled dielectric becomes larger as the aspect ratio increases, and it is especially large in structures with reentrant slopes. For a sub-half- micron vertical-profile high-aspect-ratio structure, HDP CVD of undoped oxide provides an excellent alternative to conventional LPCVD TEOS/O_2 and TEOS/O_3 processes [78]. **Figure 17** shows a 0.25-µm STI structure, having a 1.8:1 aspect ratio, filled with HDP CVD silicon oxide. It can be seen that the gap fill is excellent, and the film density is quite good. No voids were observed in the filled center, even after buffered HF highlight etching. STI structures with aspect ratios up to 3:1 have also been filled with no voids, using the HDP CVD process [45, 79]. As in the case of GC gap fill, corner erosion can be reduced with a PECVD oxide layer before HDP CVD deposition or by ramping up the rf bias (i.e., increasing the sputtering component after deposition of a thin seed layer) during the initial HDP CVD process. For STI, HDP CVD gap fill easily meets the requirement. The major issues are process integration and metal contamination.

From a process-integration viewpoint, it is more difficult to integrate the HDP CVD gap-fill process into STI process-integration schemes than the conventional LPCVD oxide deposition process. In the LPCVD oxide deposition process, the deposited film thickness and profile are more predictable and, in most cases, independent of pattern structure and density. In the TEOS/O_3 process, this pattern-density dependency becomes more complex [1]; for HDP CVD, this is one of the integration issues that will require significant effort to resolve. The pattern-density dependency in HDP CVD arises from the concurrent deposition/etching properties of the process; it has also been observed for HDP CVD gap fill of ILD structures [84]. The material deposited in the area on or near the corner and step structure is sputter-etched (by Ar^+) more readily than in a planar area. Furthermore, the deposition parameters, aspect ratios, and dimensions of the gap-fill structures also affect the amount of material deposited on surfaces, indicating that the *D/S* value of the process does not remain constant during deposition. The value changes dynamically and locally with deposited surface topography and substrate parameters during deposition.

HDP CVD films deposited over complex submicron topography structures with more holes and trenches to fill are considerably thinner than those deposited over structures containing fewer topological features. This variation can be partially reduced by two-step deposition: filling the structure partially by HDP CVD of an oxide to reduce the gap-fill aspect ratio, followed by deposition, either by PECVD of an oxide or LPCVD of an oxide. Since the planarization requirement and control of the ULSI STI process are expected to be much more stringent than those of GC and ILD structures, integration will become more difficult and will require the use of process-integration sequences similar to those mentioned in recent publications [45, 78]. Plasma damage, especially at device edges, can be eliminated by the use of a suitable process-integration scheme [45]. **Figure 18** shows multilevel 0.25-µm ULSI CMOS structures in which the STI and GC were filled with an HDP CVD oxide and subsequently planarized by CMP. It should be noted that the thickness differences over the STI structures may cause subsequent process integration problems and may result in overpolishing of STI oxide in some areas, as shown in the lower portion of the figure. STI structures having 0.17-µm dimensions and up to a 3.5:1 aspect ratio have also been deposited with HDP CVD oxide films with no voids [45]. It can thus be seen that good gap fill and planarization can be achieved with HDP CVD processing for sub-half-micron STI with suitable process integration.

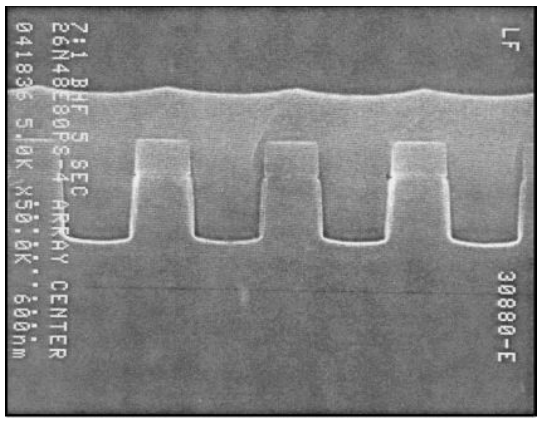

Figure 17

SEM cross-section micrograph illustrating gap filling and local planarization of a shallow-trench isolation structure, achieved using HDP CVD of silicon oxide.

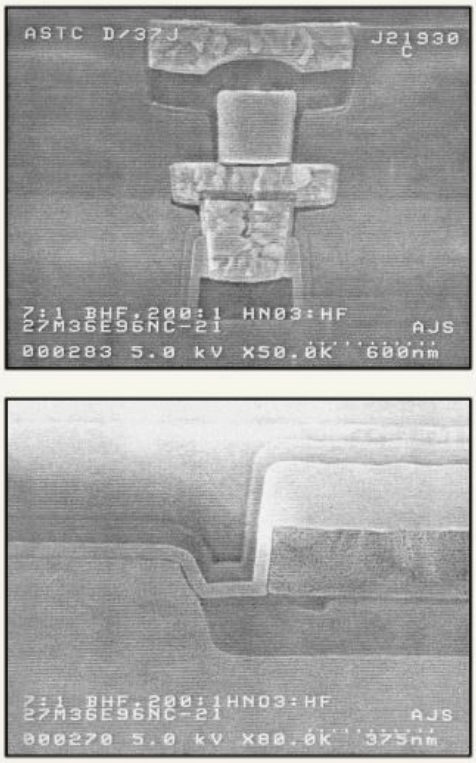

Figure 18

SEM cross-section micrographs of multilevel 0.25-μm ULSI structures in which gap filling and coating were achieved by HDP CVD of silicon oxide followed by CMP.

If there is one critical problem that will prevent the use of HDP CVD silicon oxide films in STI gap-fill applications, it is metal contamination. For ULSI STI applications, only a small level of metal contamination (>1 x 10^{15} cm^{-3}) in deposited films will cause unwanted diffusion in subsequent high- temperature (850-1000°C) annealing steps, and deleteriously affect device performance. For mobile ions such as Na^+ and Li^+, the contamination threshold may have to be even lower. As mentioned before, the high-density plasma Ar^+ sputtering required for high-aspect-ratio gap fill will also sputter off the metals (Al, Fe, Ni) from the alumina domes that are currently used in most commercial ICP HDP CVD reactors and cause subsequent metal contamination in deposited films. The high-rate, high-energy fluorine-based plasma-cleaning step for the HDP CVD reaction after deposition may also cause (minuscule amounts of) metal contamination in the reactor and subsequently in the deposited STI oxide films. If HDP CVD silicon oxide is used for ULSI STI fabrication in manufacturing, various metal-

contamination monitors and process controls will have to be implemented to ensure that the contamination is consistently below acceptable levels. A recent study [32] has shown that the mobile ion level in advanced HDP CVD systems can be consistently maintained at relatively low levels. However, even at these levels the contamination is still higher than those of LPCVD TEOS/O_2 and may be unacceptable for sub-0.25-µm STI oxide gap-fill dielectric applications. Whether this level of metal contamination can be reduced further and/or maintained at sufficiently low levels during deposition in an HDP CVD system and deposited films will probably be one of the factors which determine whether the HDP CVD oxide gap-fill process will be used for future STI applications.

Summary

In this paper, we have presented and reviewed recent developments in the HDP CVD of silicon oxide, fluorine-doped silicon oxide, and other carbon and fluorocarbon low-dielectric-constant films of current interest in integrated- circuit fabrication. Dielectric films deposited by HDP CVD processing not only have better gap-fill properties but also have improved physical, chemical, and electrical properties compared to those produced by the conventional plasma CVD process. For IMD applications, the HDP CVD of silicon oxide has performance and cost advantages, and has been implemented for forming IMD dielectrics in IBM sub-half-micron ULSI CMOS manufacturing. Significant progress has also been made in the HDP CVD of fluorinated silicon oxide. With regard to HDP CVD silicon oxide and PGS film applications to shallow-trench isolation (STI) and gate-conductor (GC) gap fill, issues pertaining to metal contamination and process integration continue to be of concern. HDP CVD carbon and fluorocarbon films may be useful in conjunction with low-*k* objectives, but it may be less costly to use conventional plasma CVD for depositing such films. Nevertheless, the results covered in this paper suggest that if the metal-contamination and process-integration concerns can be effectively addressed, the HDP CVD process may play an important role in the future fabrication of integrated circuits.

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